

Compal Confidential

KALG1 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-03-02

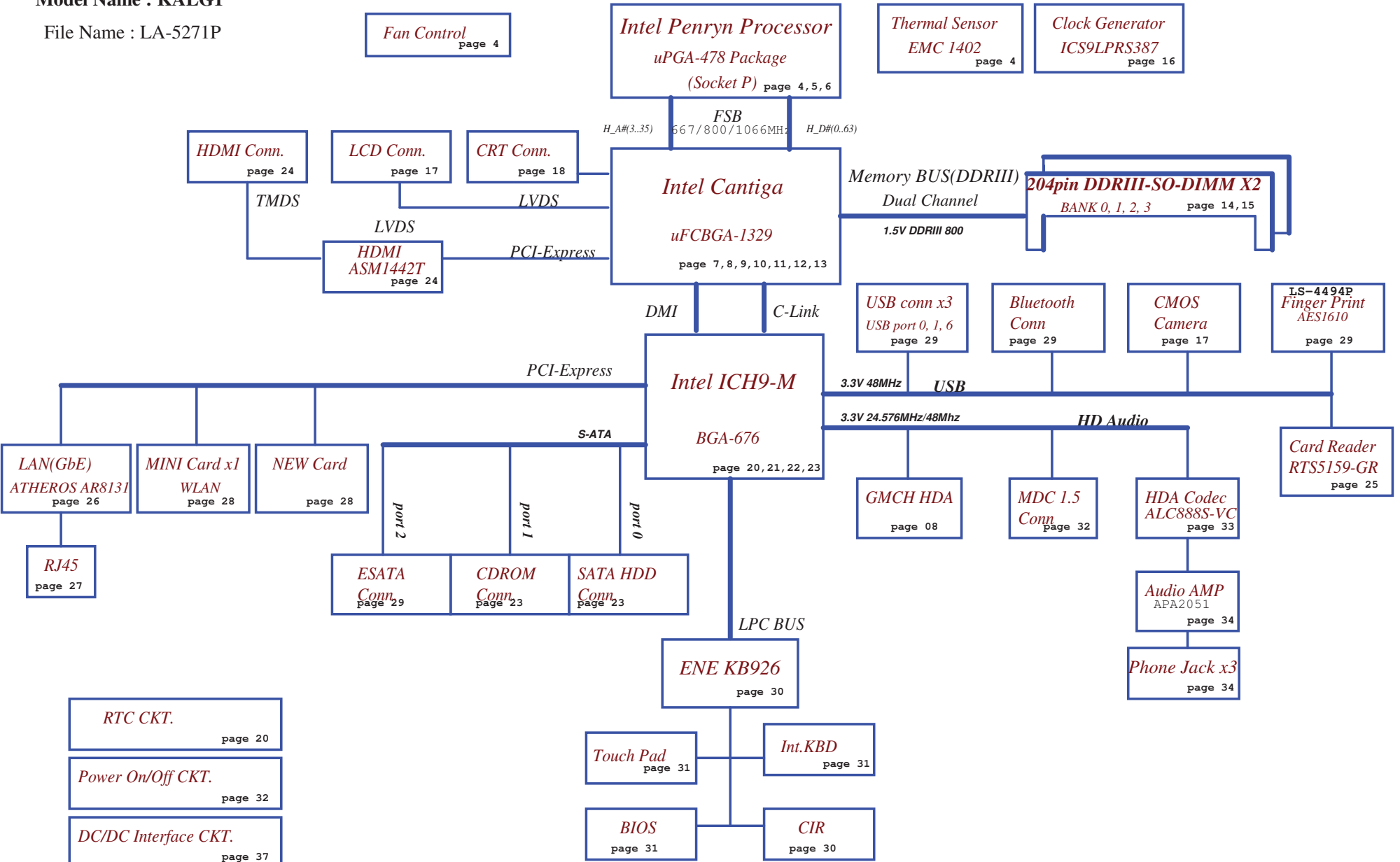
REV 02

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				Date: Tuesday, March 24, 2009	Sheet 1 of 45

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Model Name : KALG1

File Name : LA-5271P



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				KALG1	0.1
				Date: Tuesday, March 24, 2009	Sheet 2 of 45

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75VS power rail for DDR3 terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for NB(LVDS)	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3V	3.3V power rail for SB	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail for SB	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR3 DIMMA	1001 000Xb
DDR3 DIMMB	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1				
2				
3				
4				
5				
6				
7				

BOARD ID Table




Board ID	PCB Revision
0	PCB 08Y LA-5271P REV0 M/B
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

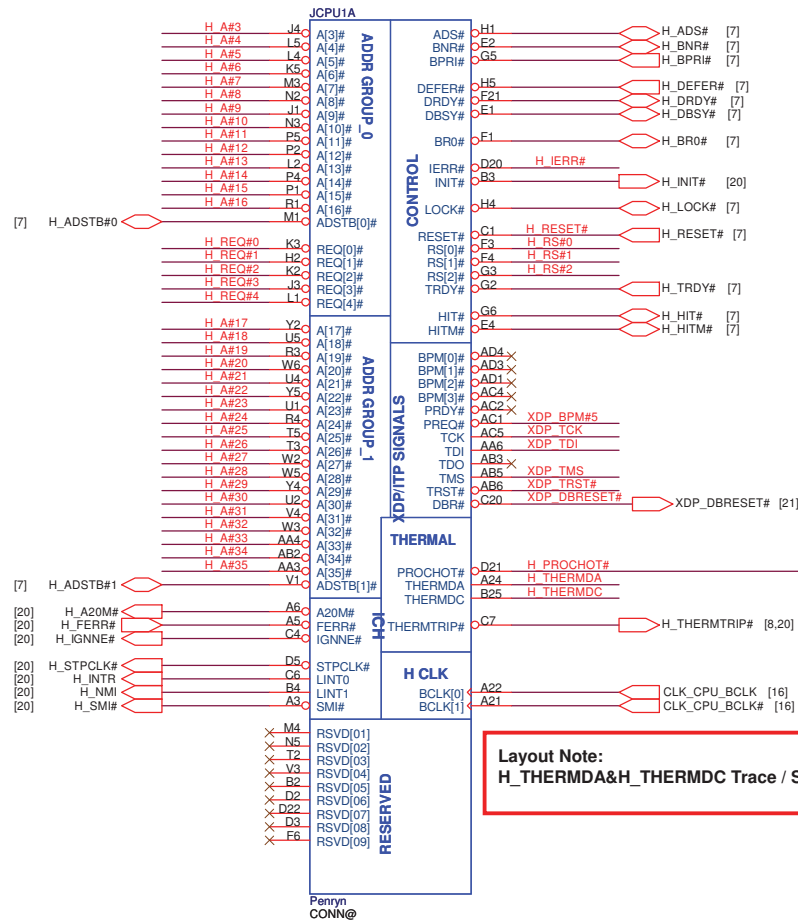
BTO Item	BOM Structure
GL40	GL40@
GM45	GM45@

BOM Configuration Table

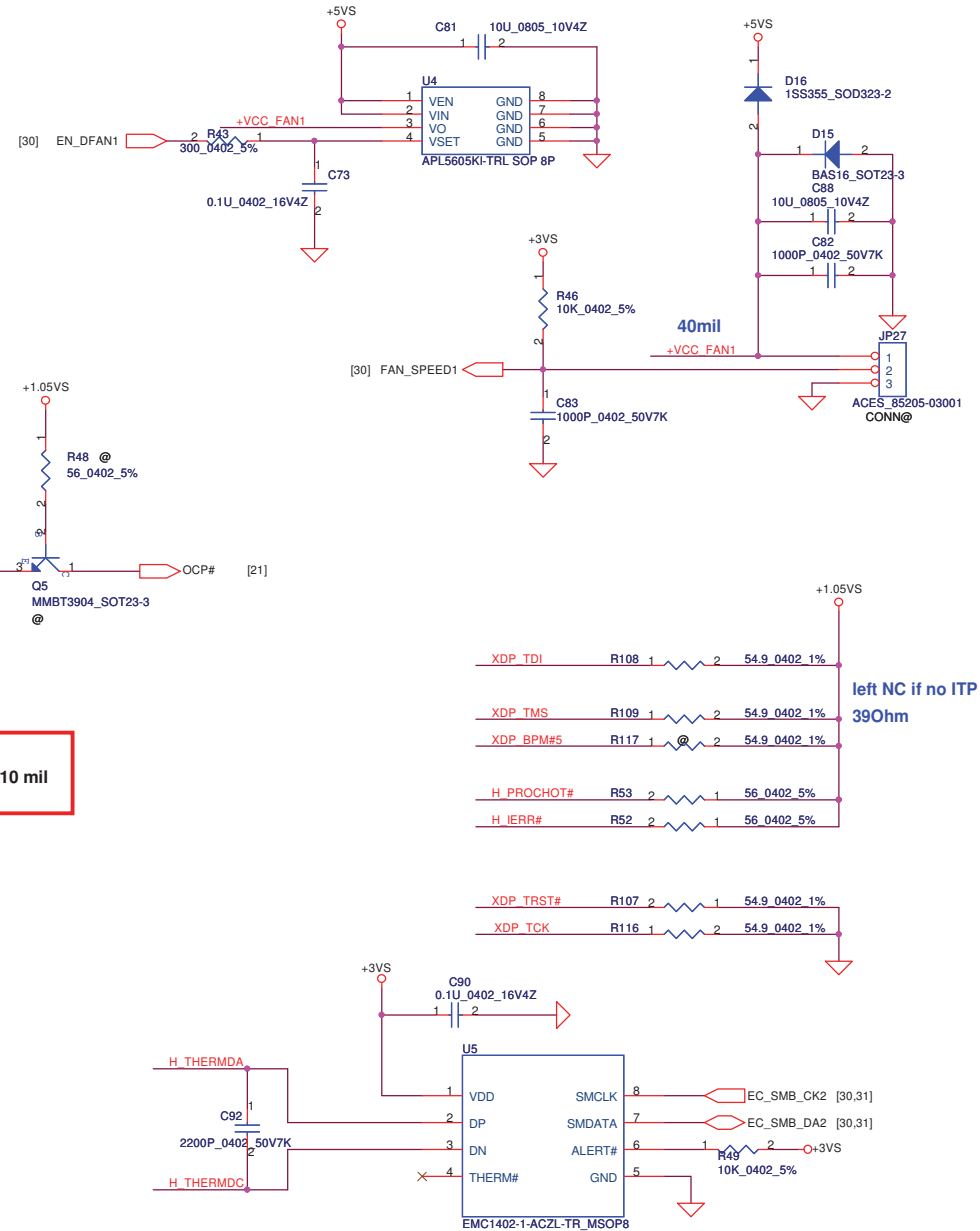
Project	BOM Configuration
KALG1-GM45	GM45@/KALG1@/KAL90_G0_90+@
KALG1-GL40	GL40@/KALG1@/KAL90_G0_90+@

[7] H_A# [3..35]  H_A# [3..35]
 [7] H_REQ# [0..4]  H_REQ# [0..4]
 [7] H_RS# [0..2]  H_RS# [0..2]

FAN1 Conn



Layout Note:
 H_THERMDA & H_THERMDC Trace / Space = 10 / 10 mil



BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

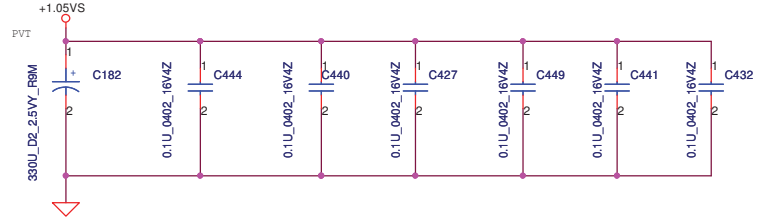
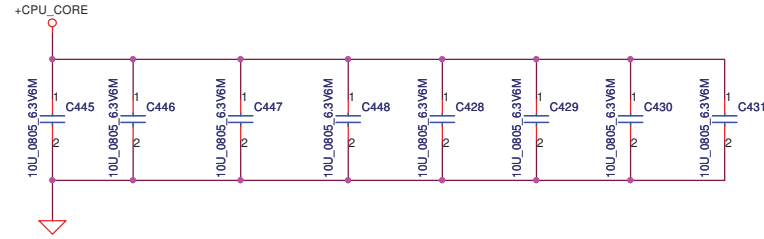
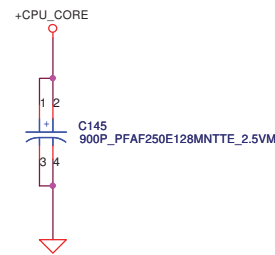
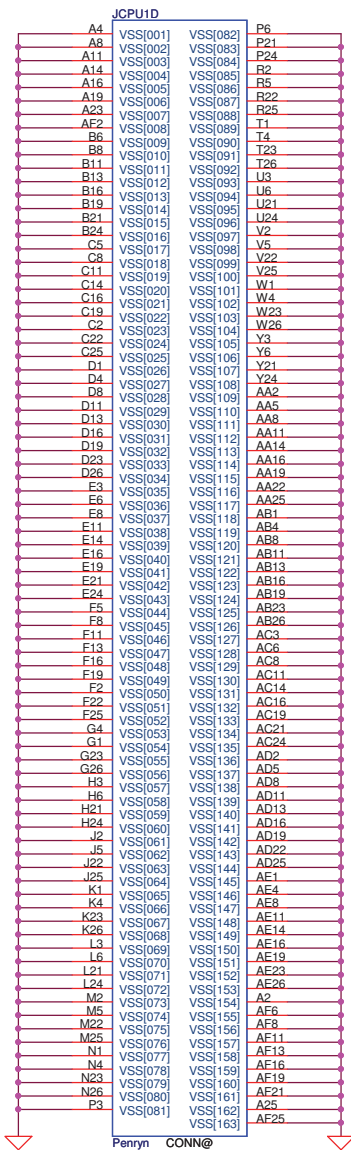
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						Size B	Document Number			Rev		
						KALG1				0.1		
						Date:	Tuesday, March 24, 2009		Sheet	4	of	45

Trace Close CPU < 0.5'
Width=4 mil,
Spacing: 15mil
(55Ohm)

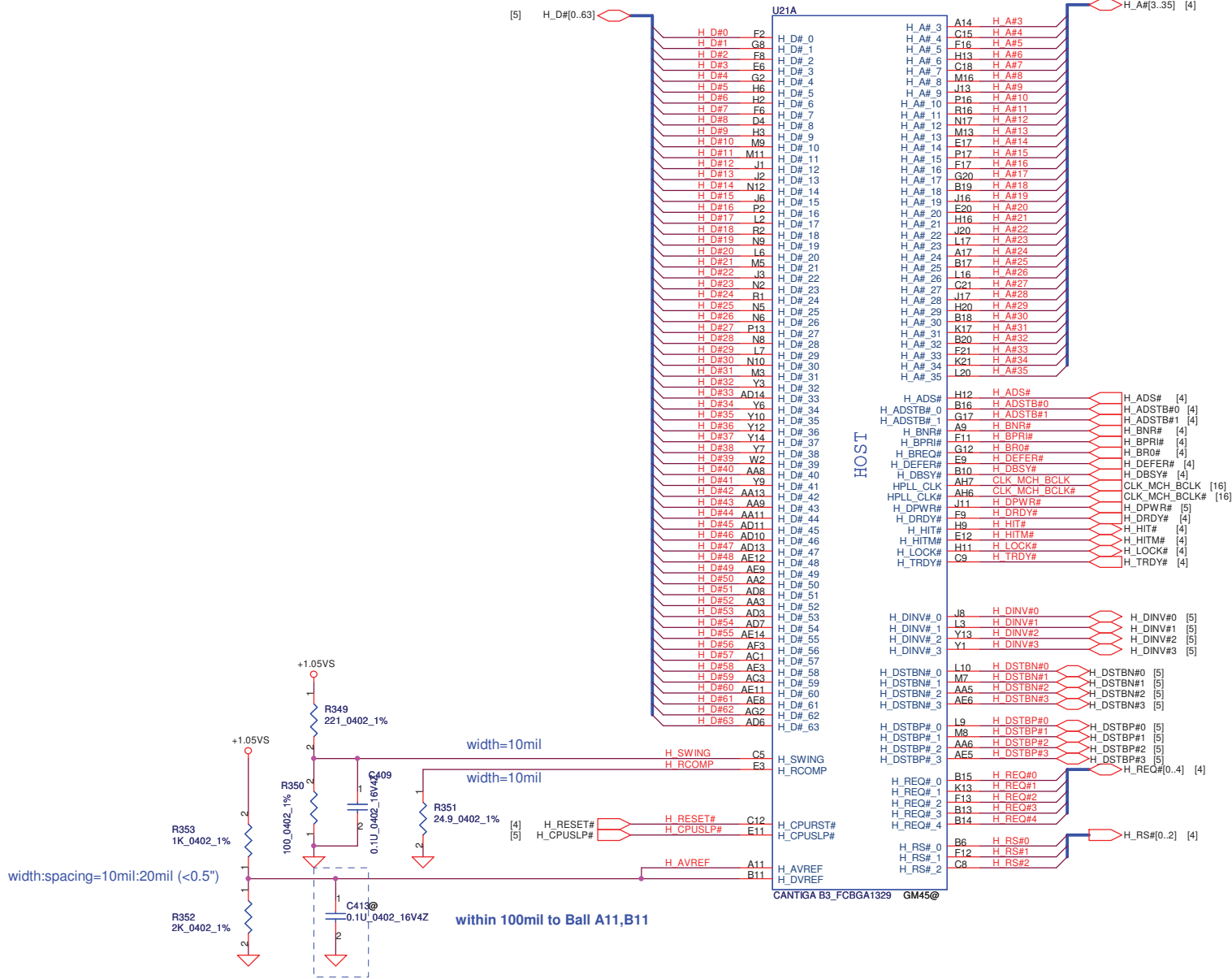
TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 16mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

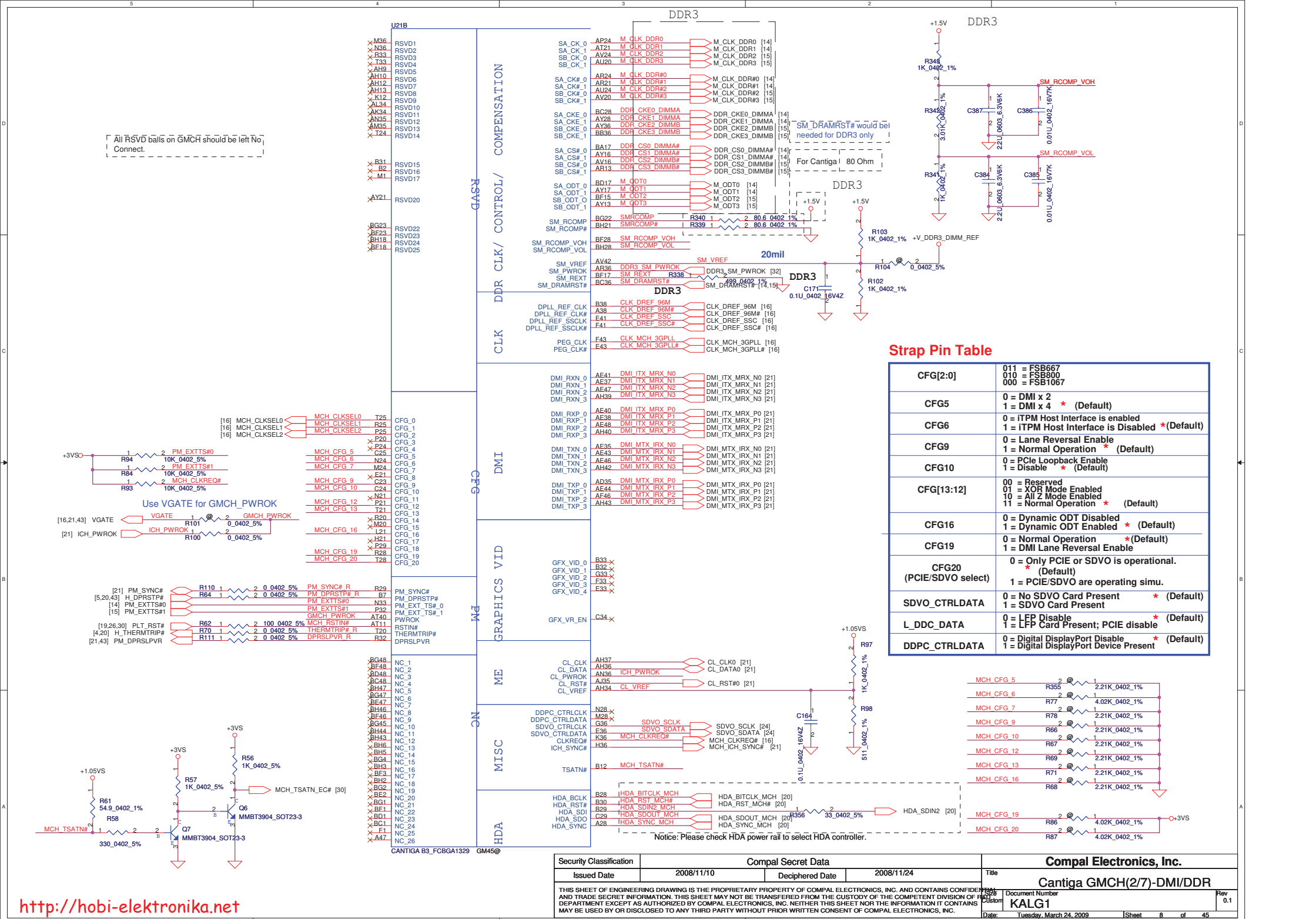
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Size B	Document Number	KALG1		Rev	0.1
Date:	Tuesday, March 24, 2009	Sheet	5	of	45



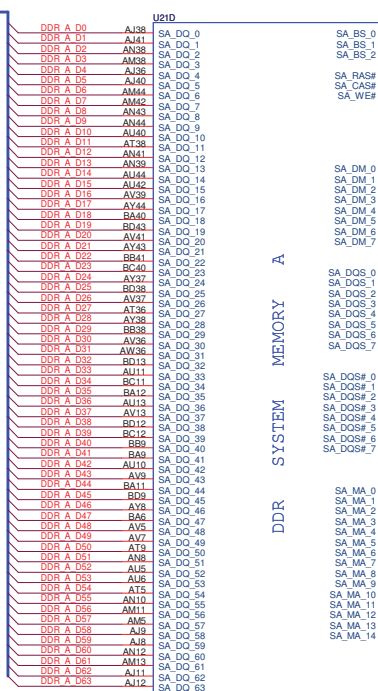
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						B	KALG1			0.1			
						Date:	Tuesday, March 24, 2009			Sheet	6	of	45



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Size B	Document Number	KALG1		Rev	0.1
Date:	Tuesday, March 24, 2009	Sheet	7	of	45

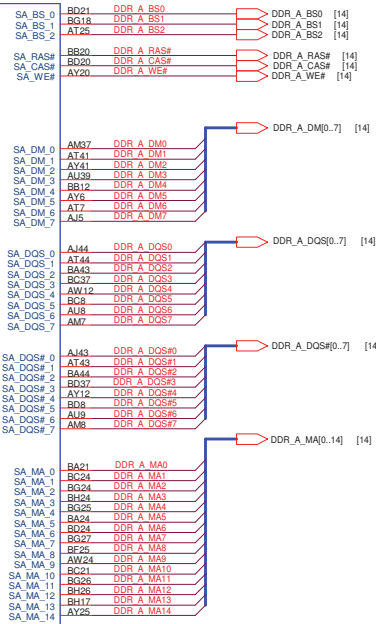


[14] DDR_A_D[0..63]



CANTIGA B3_FCBGA1329 GM45@

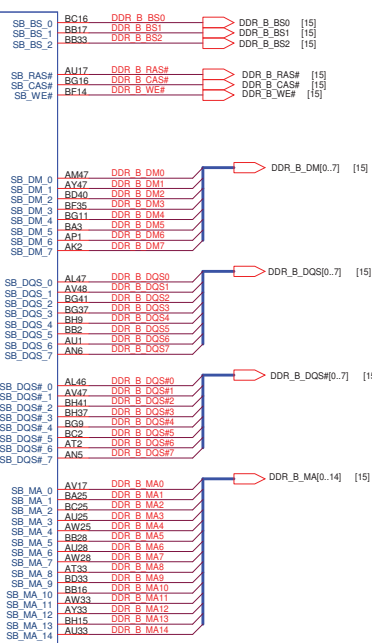
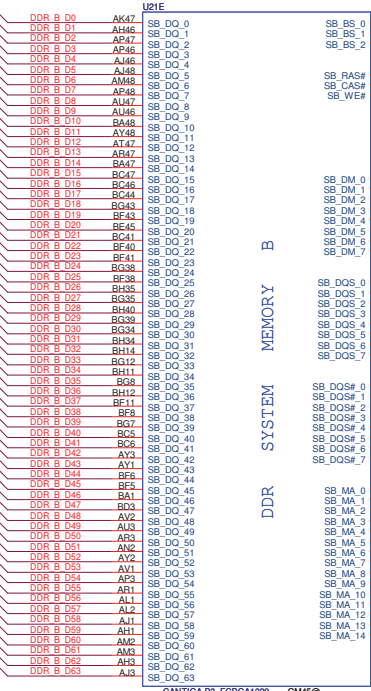
DDR SYSTEM MEMORY A



CANTIGA B3_FCBGA1329 GM45@

DDR SYSTEM MEMORY B

[15] DDR_B_D[0..63]

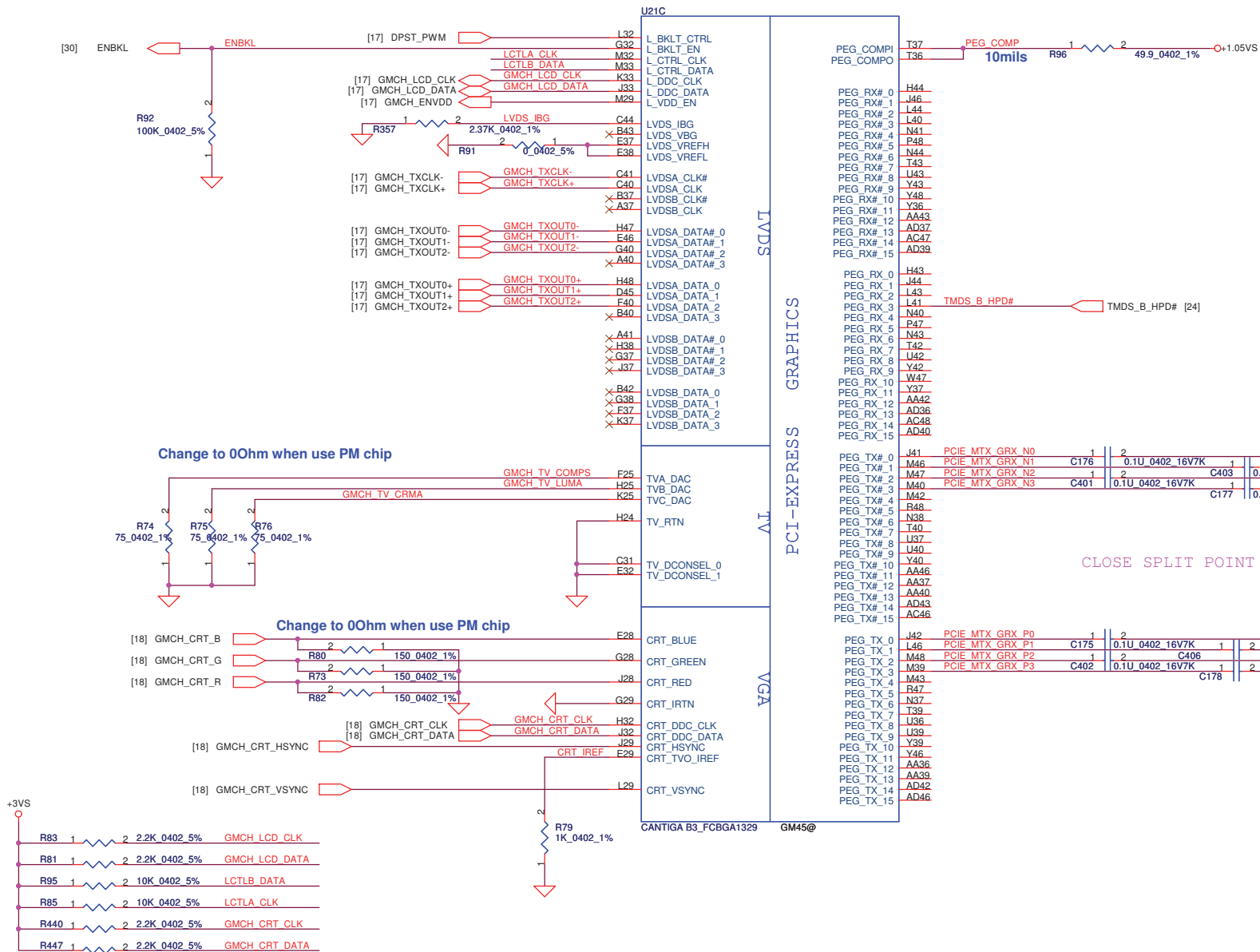


Compal Electronics, Inc.

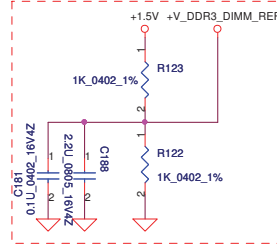
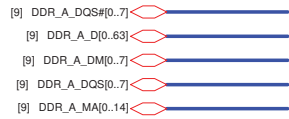
Cantiga GMCH(3/7)-DDR

Size	Document Number	Rev
C	KALG1	0.1
Date:	Tuesday, March 24, 2009	Sheet 9 of 45

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Issued Date	2008/11/10
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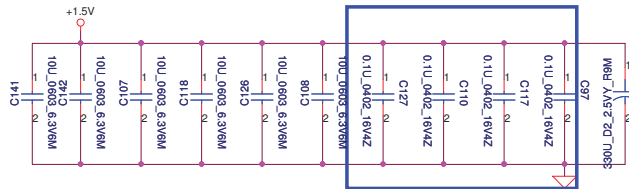


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Size	Custom	Document Number	KALG1	Rev	0.1
Date:	Tuesday, March 24, 2009	Sheet	10	of	45

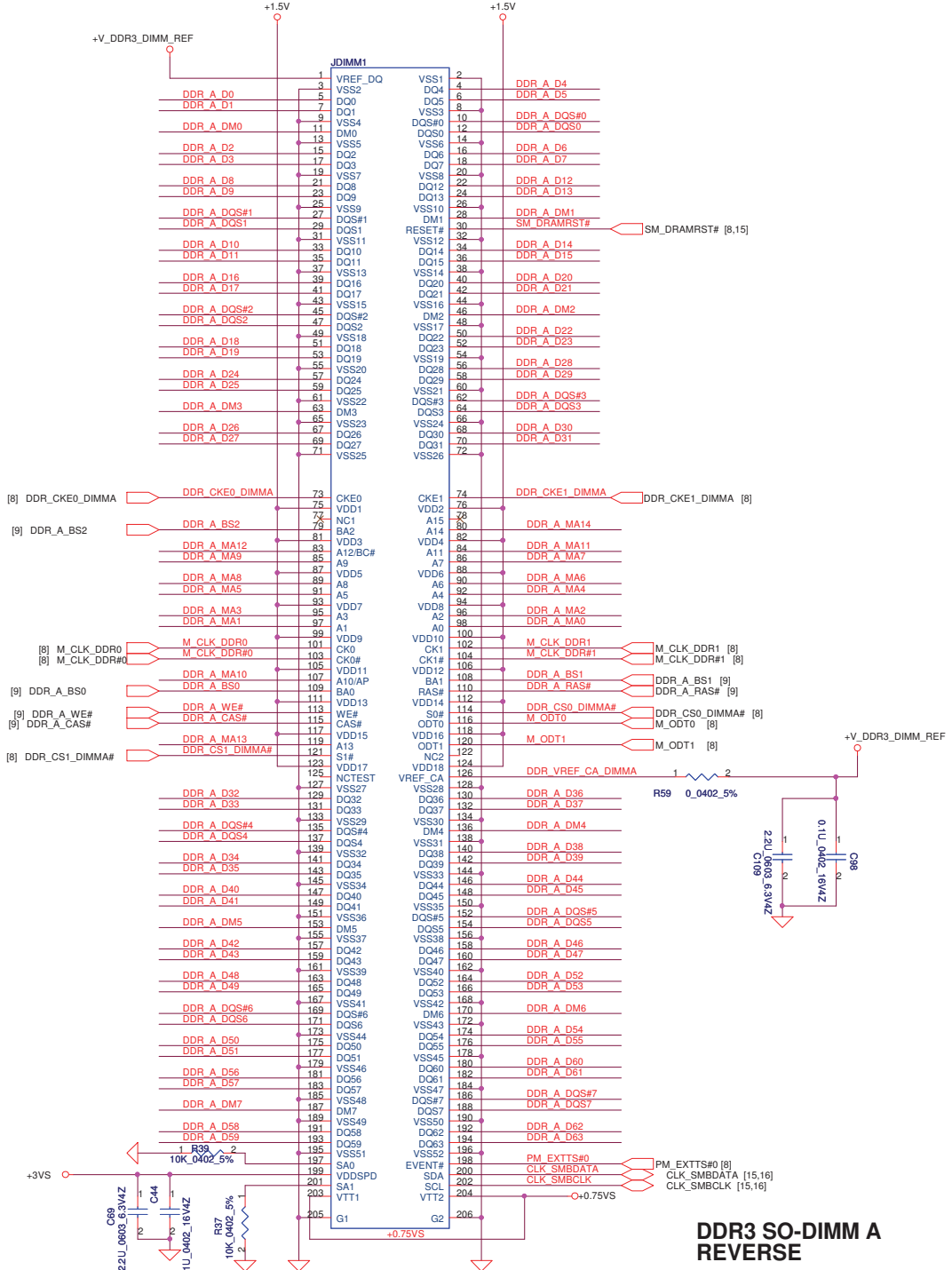
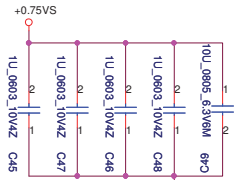


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA

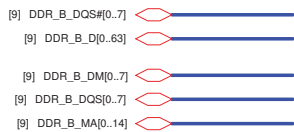


Layout Note:
Place near JP4.203 & JP4.204



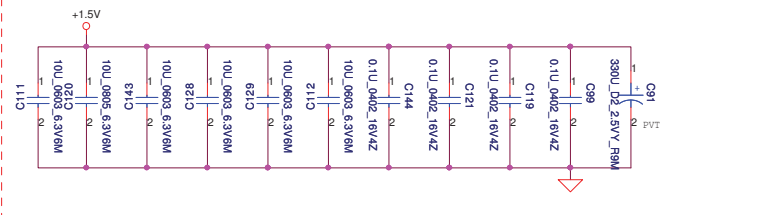
DDR3 SO-DIMM A REVERSE

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Date: Tuesday, March 24, 2009				Sheet 14 of 45

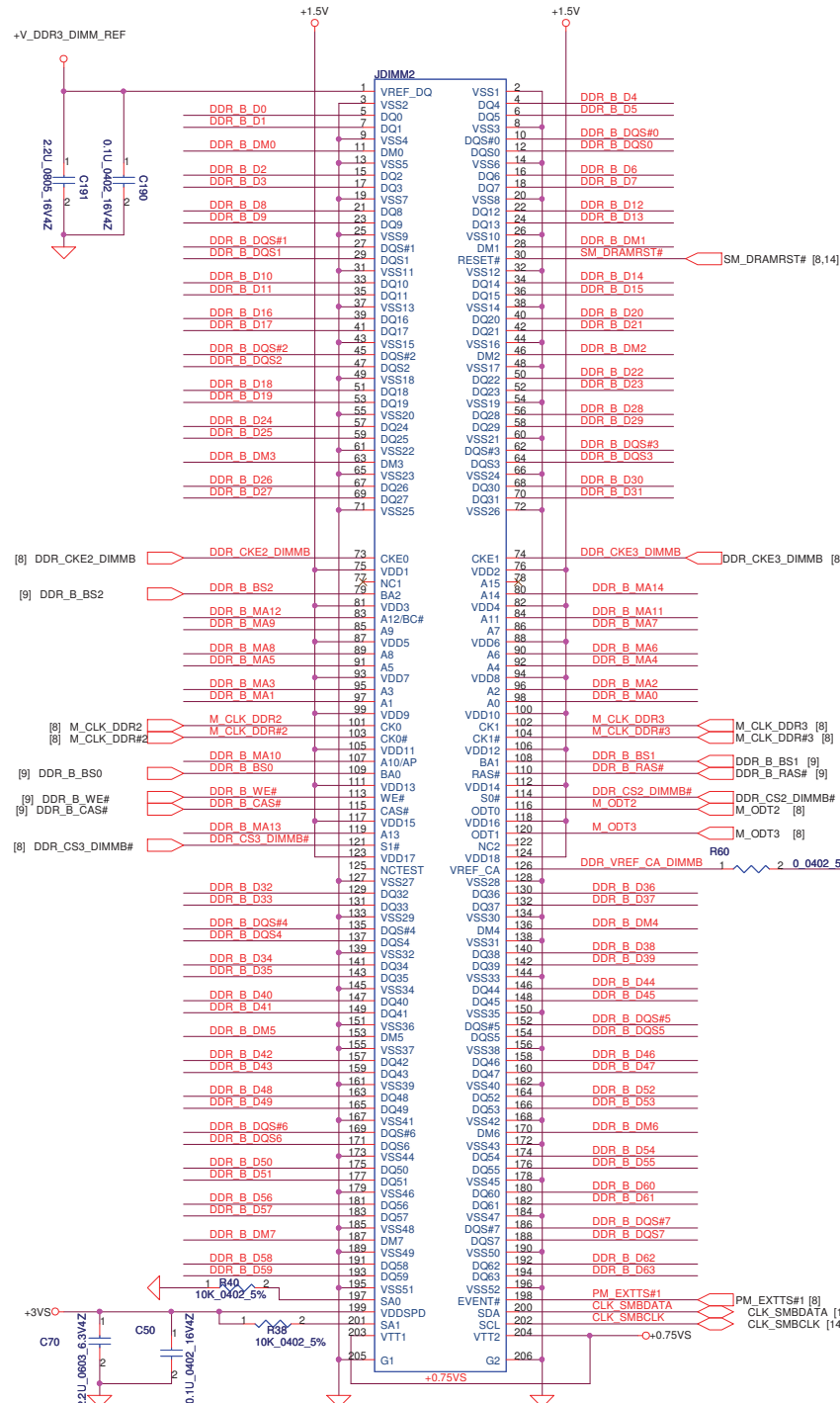
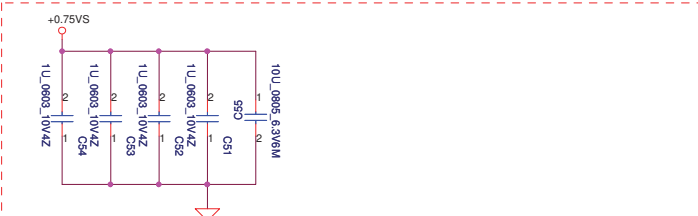


Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMB



Layout Note:
Place near JP5.203 & JP5.204



**DDR3 SO-DIMM B
REVERSE**

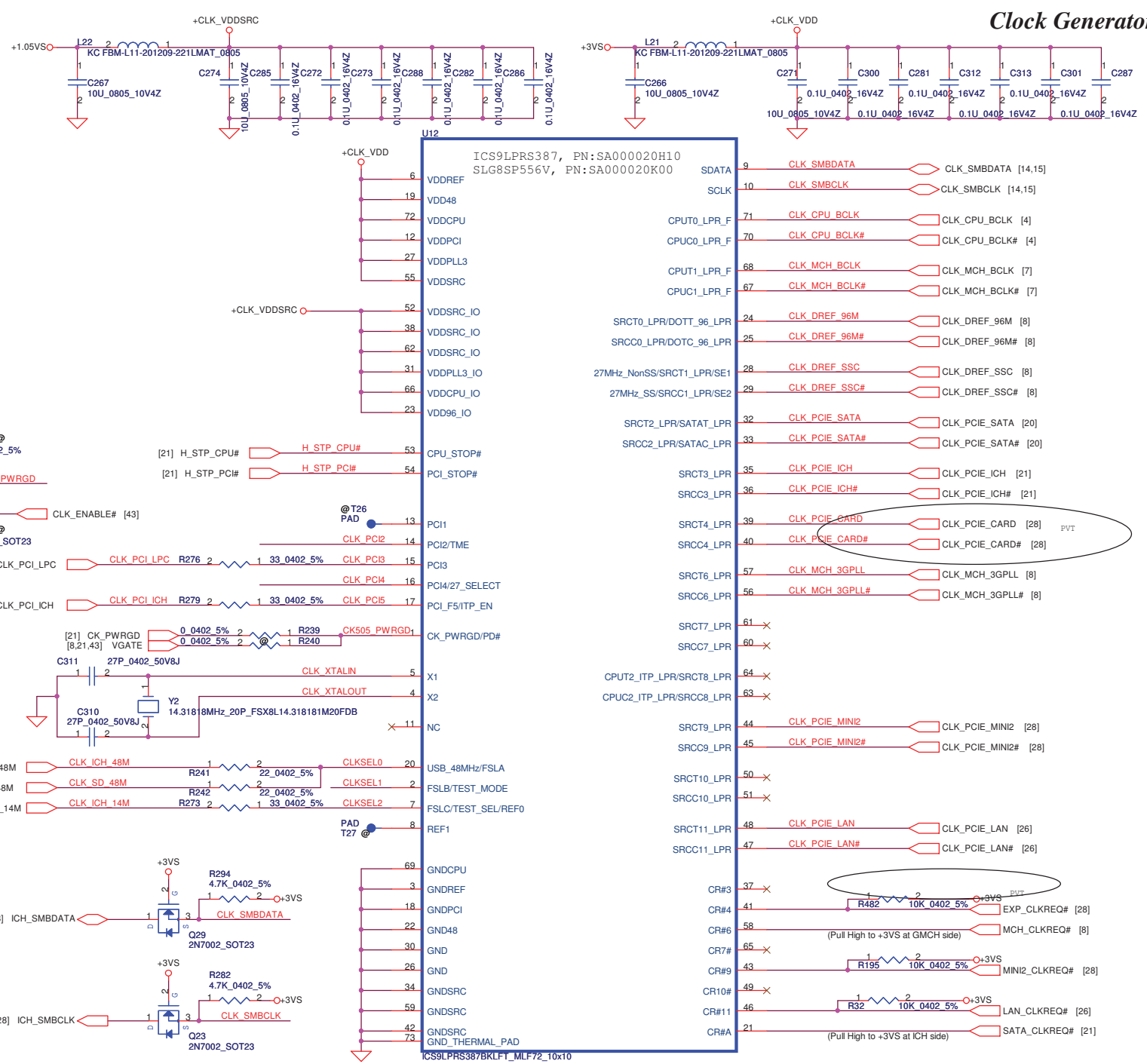
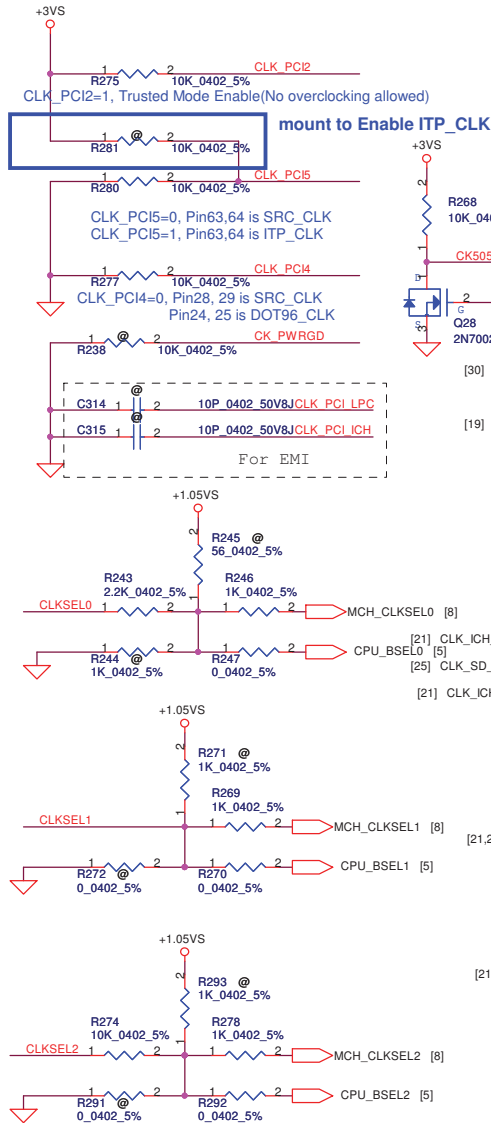
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KALGI				Document Number	Rev 0.1
Date: Tuesday, March 24, 2009				Sheet	15 of 45

FSLC	FSLB	FSLA	CPU MHz	SRC MHz	PCI MHz
CLKSEL2	CLKSEL1	CLKSEL0			
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

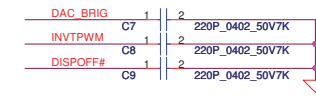
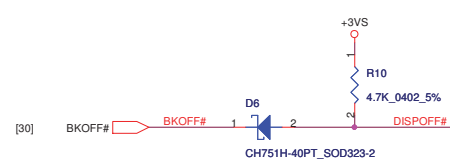
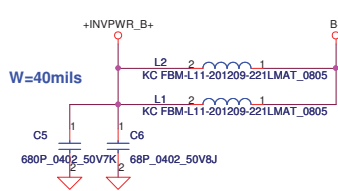
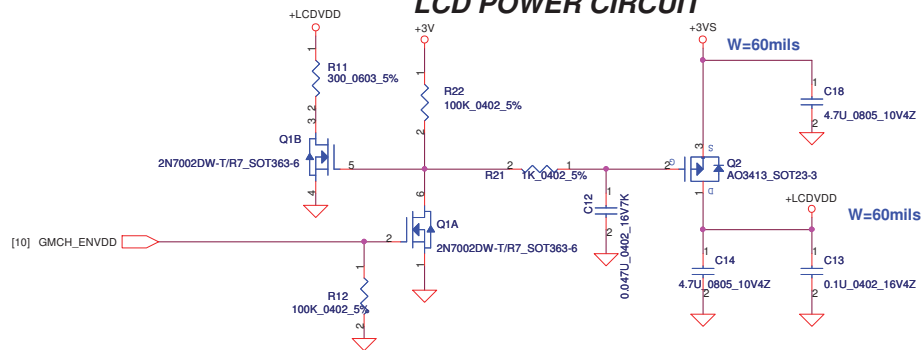
SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]



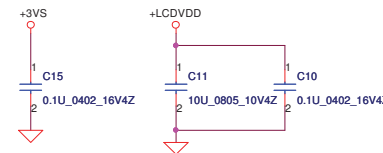
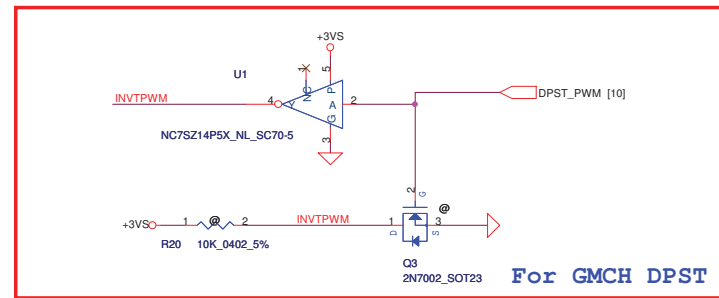
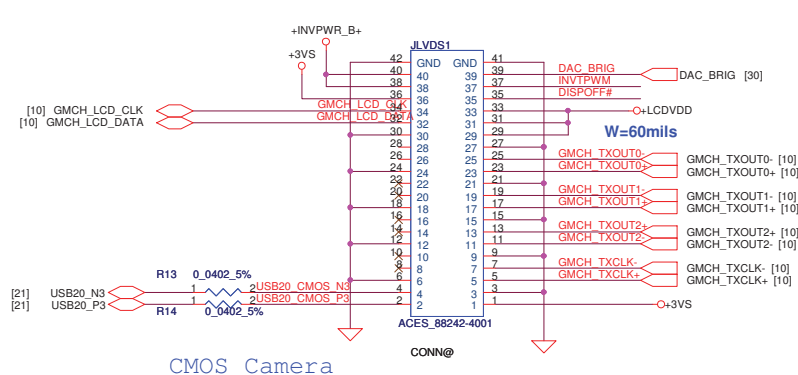
Clock Generator

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2008/11/10				2008/11/24				Title			
2008/11/24				Clock Generator (CK505)				Size			
Custom				KALG1				Document Number			
Date: Tuesday, March 24, 2009				Sheet 16 of 45				Rev 0.1			

LCD POWER CIRCUIT

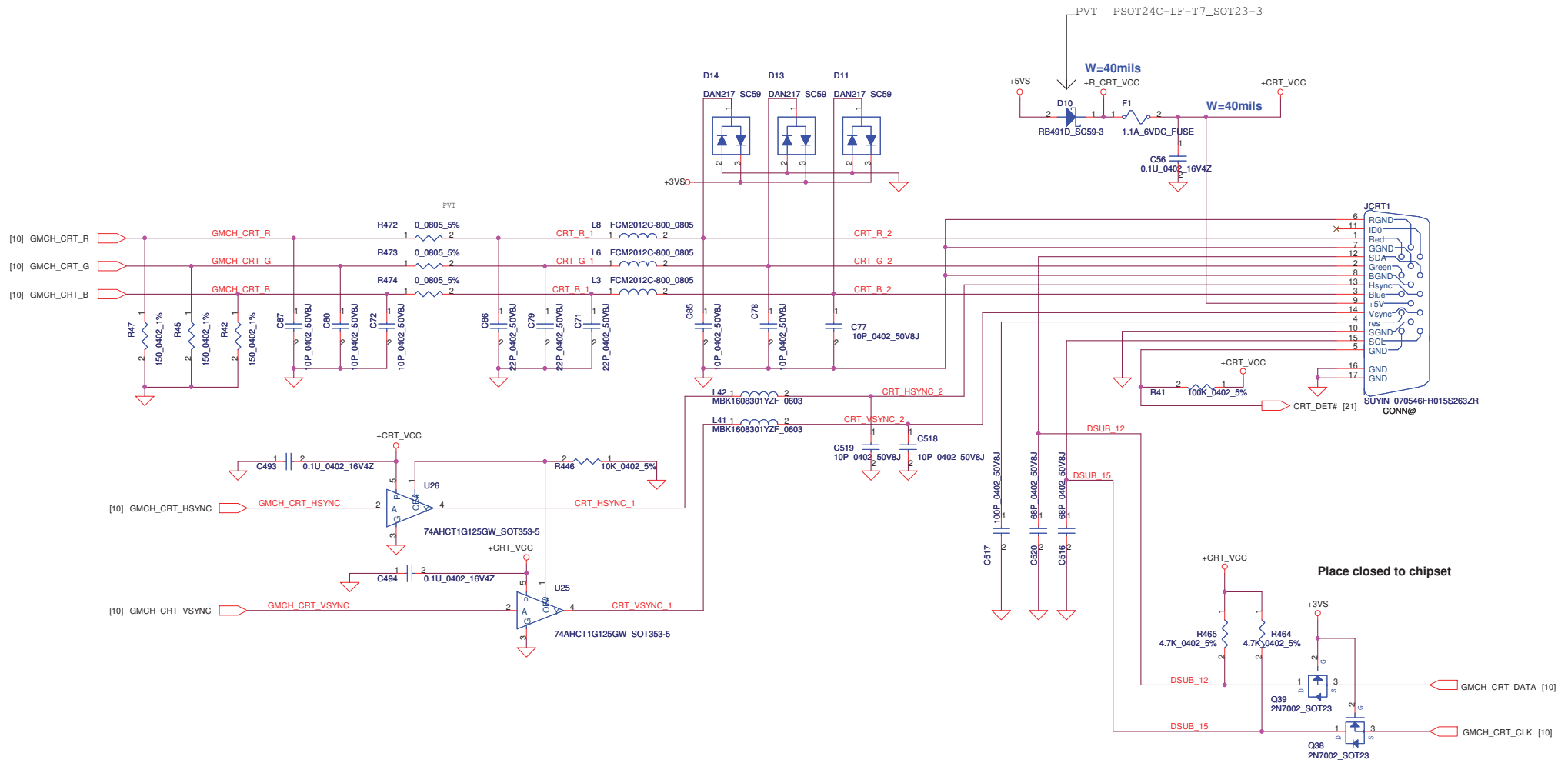


LCD/PANEL BD. Conn.

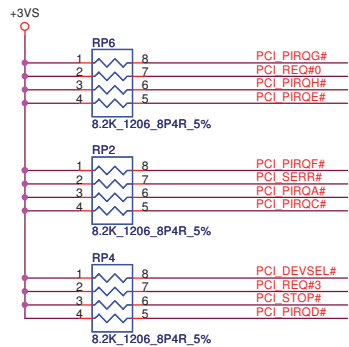
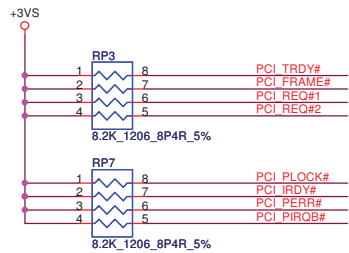


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KALG1		KALG1		0.1	
Date: Tuesday, March 24, 2009		Sheet		17 of 45	

CRT Connector

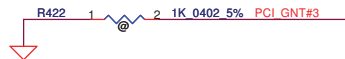


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Date: Tuesday, March 24, 2009		Sheet 18 of 45			

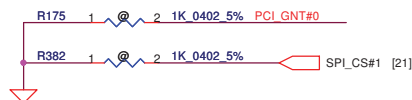


A16 Swap Override Strap

PCI_GNT#3 Low= A16 swap override Enable
High= Default*

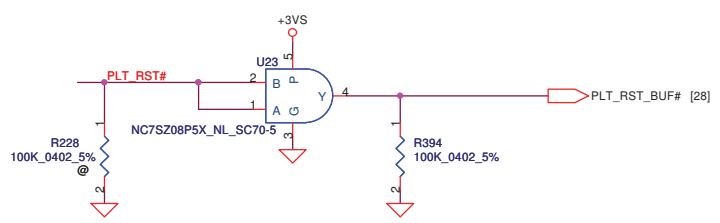
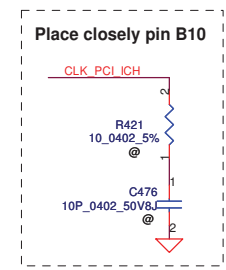
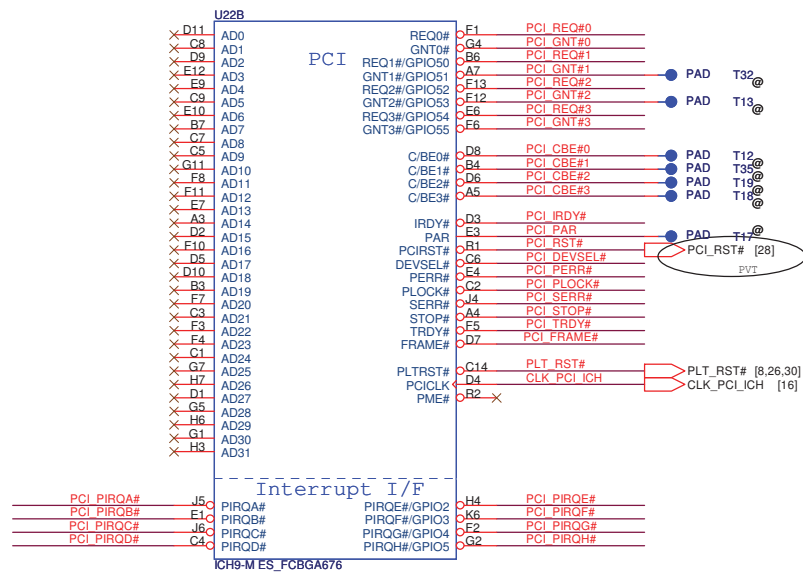


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



DMI for ESI-compatible operation

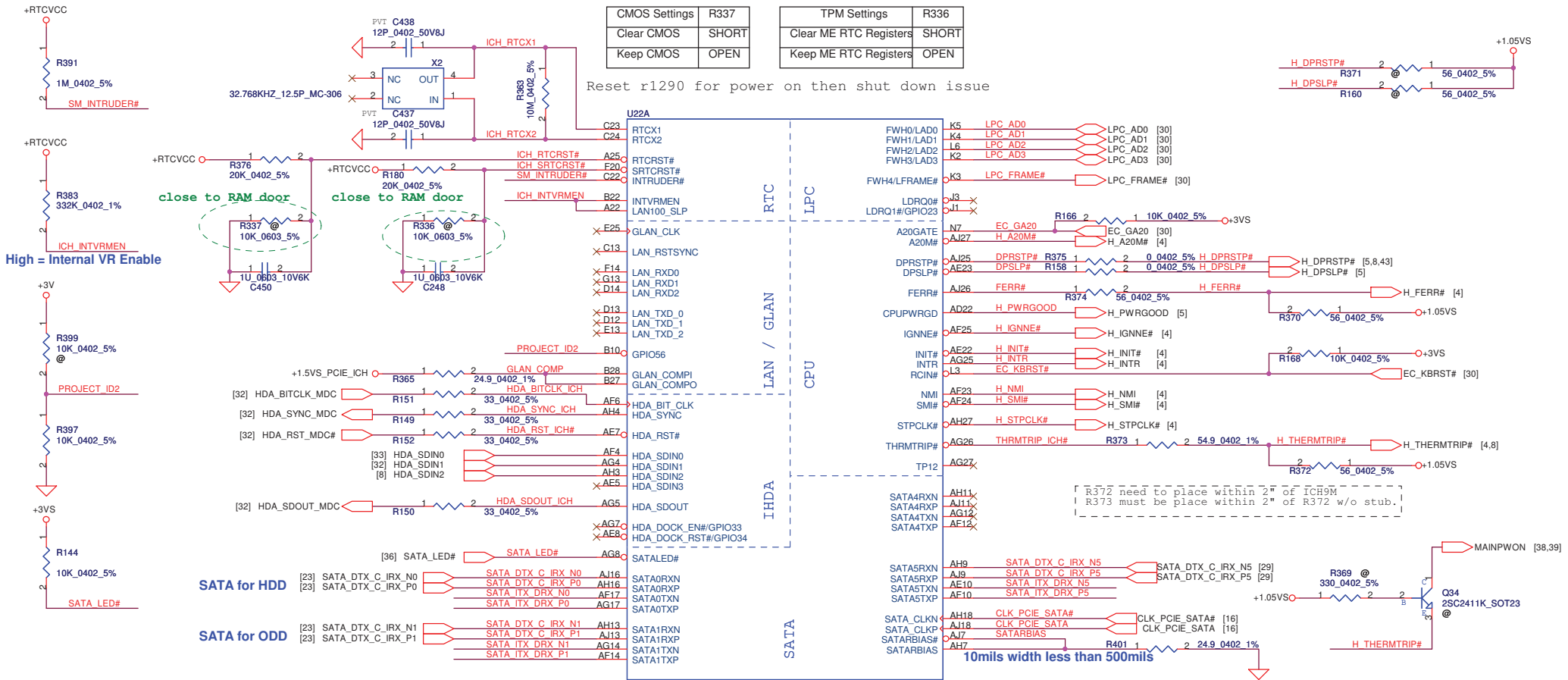
PCI_GNT#1 Low= DMI for ESI-compatible operation
High= Default* (Internal pull-up)



CMOS Settings	R337
Clear CMOS	SHORT
Keep CMOS	OPEN

TPM Settings	R336
Clear ME RTC Registers	SHORT
Keep ME RTC Registers	OPEN

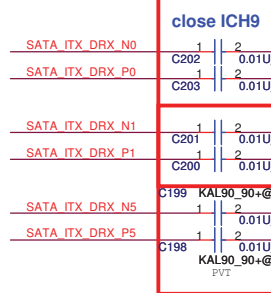
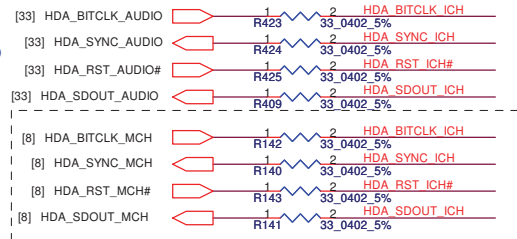
Reset r1290 for power on then shut down issue



PROJECT_ID	ID0	ID1	ID2
KAL90	0	0	0
KAL90+	1	0	0
KALG1	0	1	0
KALG0	1	1	0

HDA for AUDIO

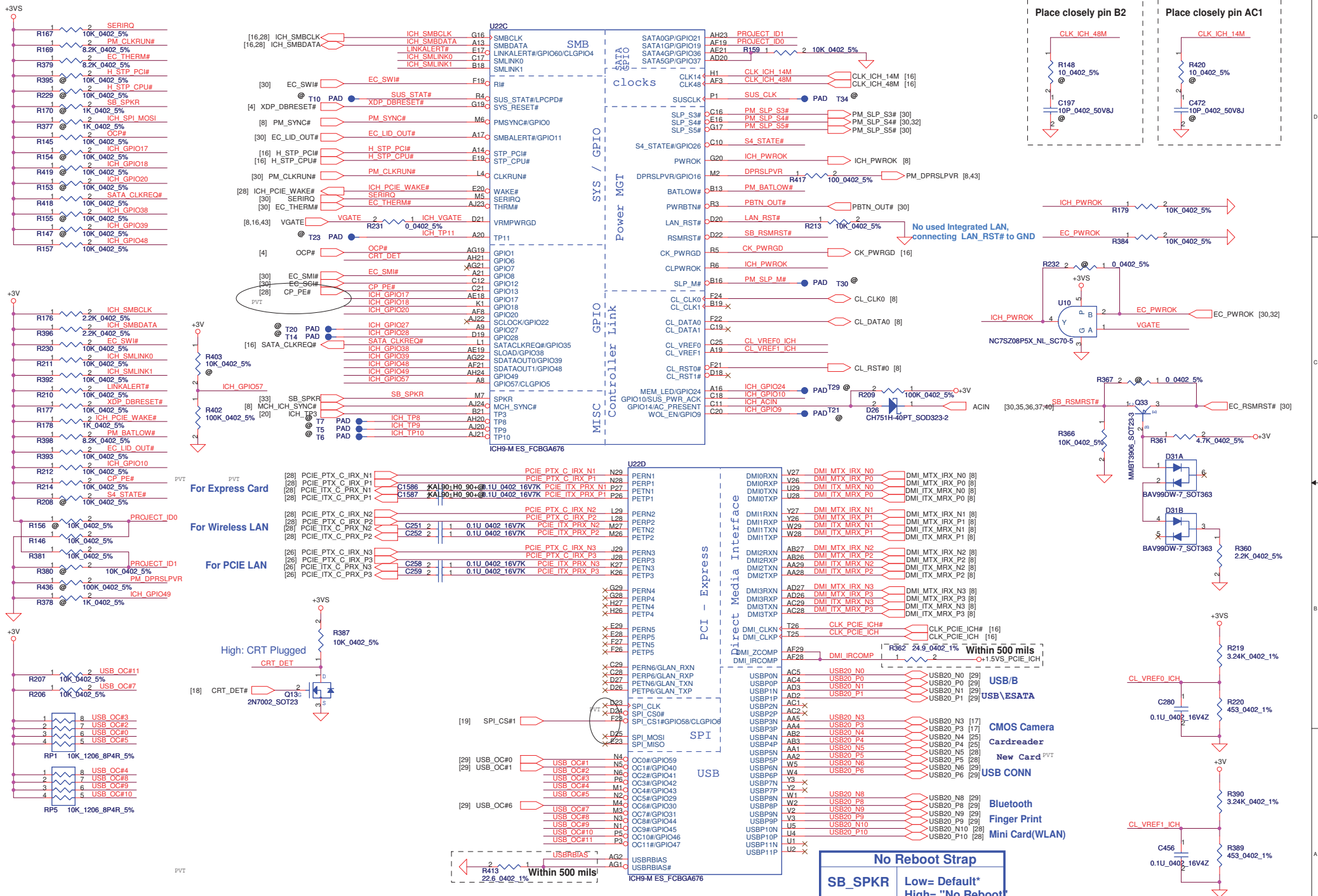
HDA for GMCH



Flash Descriptor Security Override Strap
GPIO33 Low= Descriptor Security override
High= Default* (Internal pull-up)

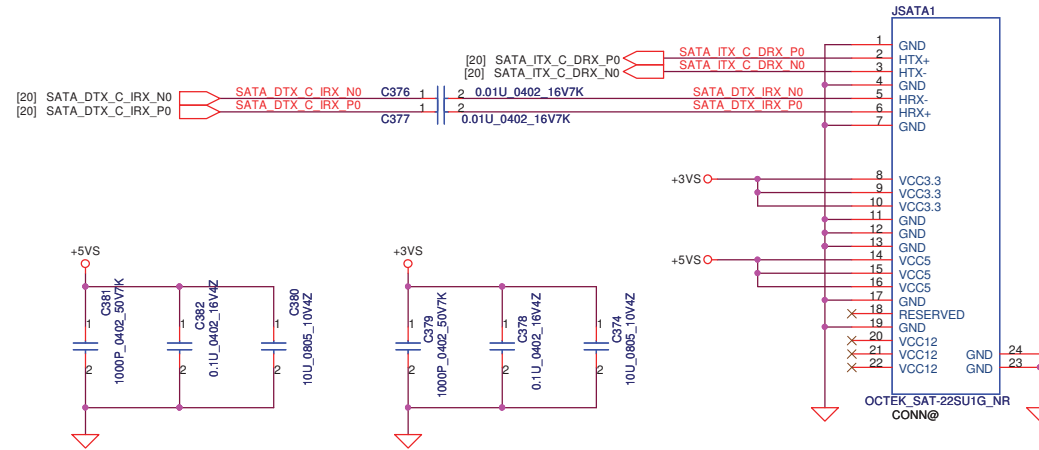
XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIe port config bit 1

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Size Custom	Document Number KALG1	Rev 0.1	
Date	Tuesday, March 24, 2009	Sheet	20 of 45

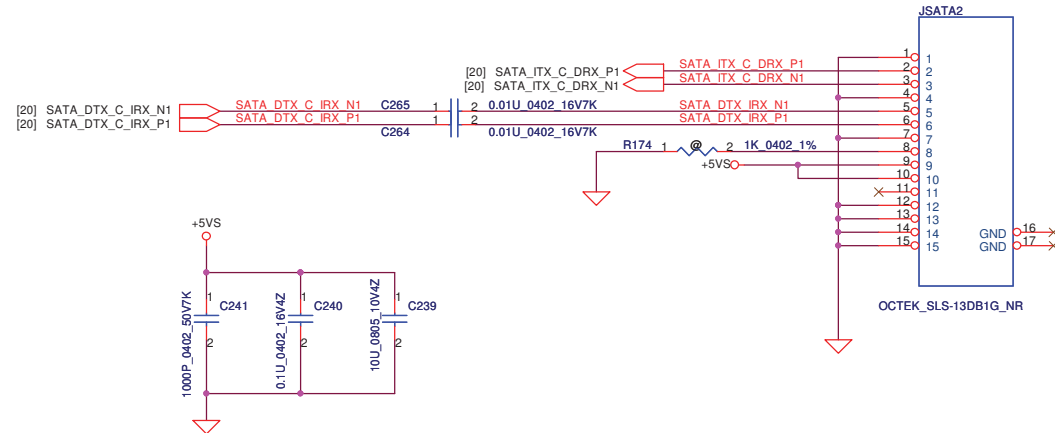




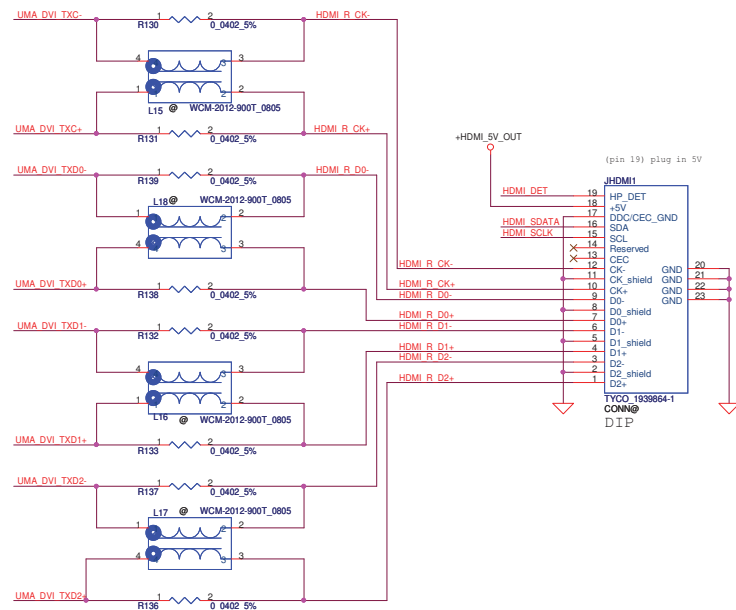
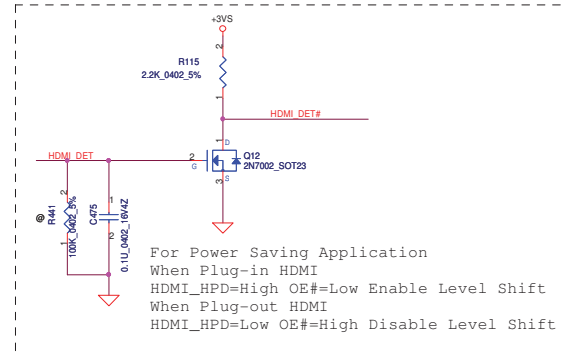
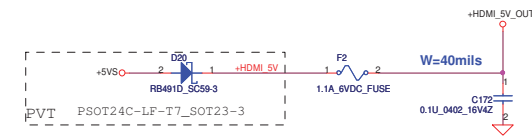
SATA HDD Conn.



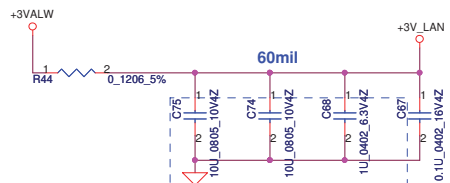
SATA ODD Conn.



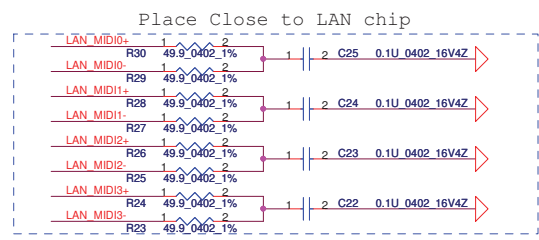
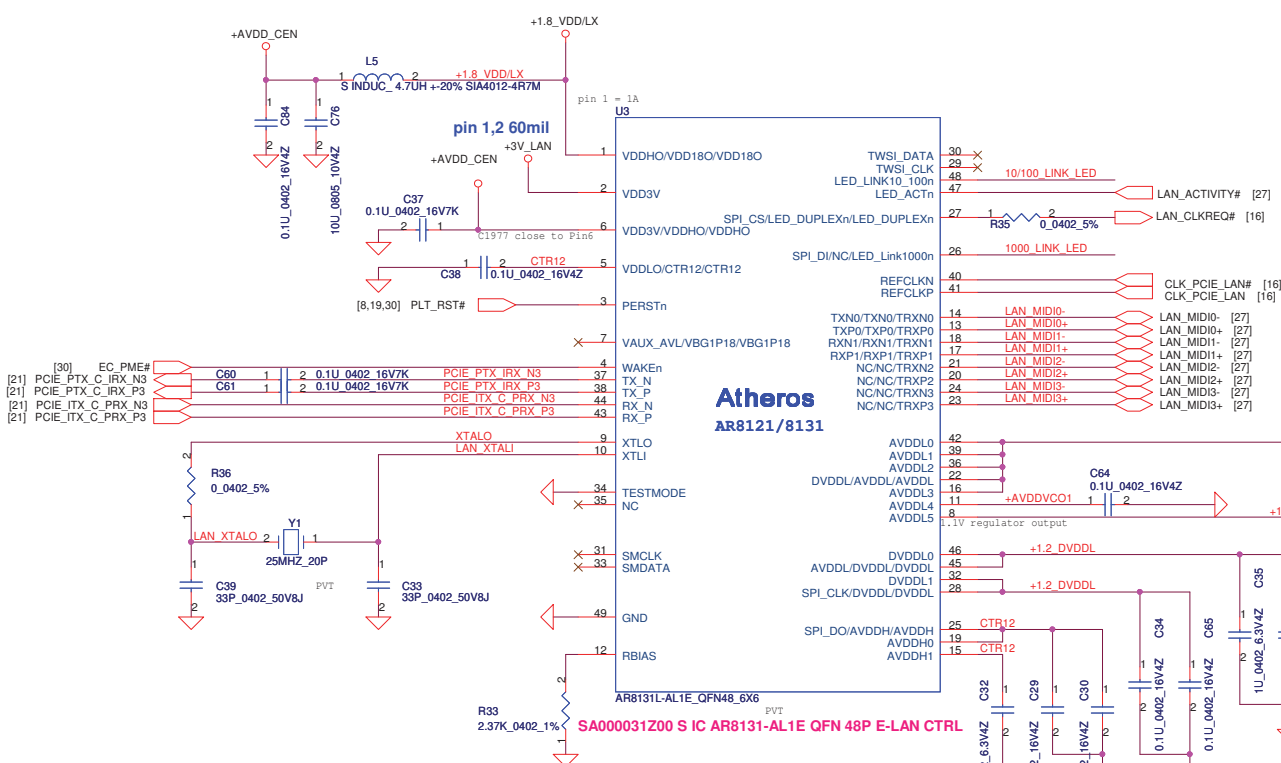
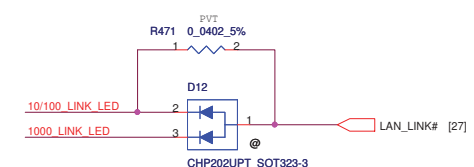
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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	
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Size	Custom	Document Number	KALG1	Rev	0.1
Date:	Tuesday, March 24, 2009	Sheet	23	of	45



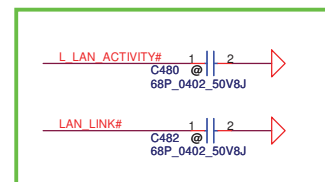
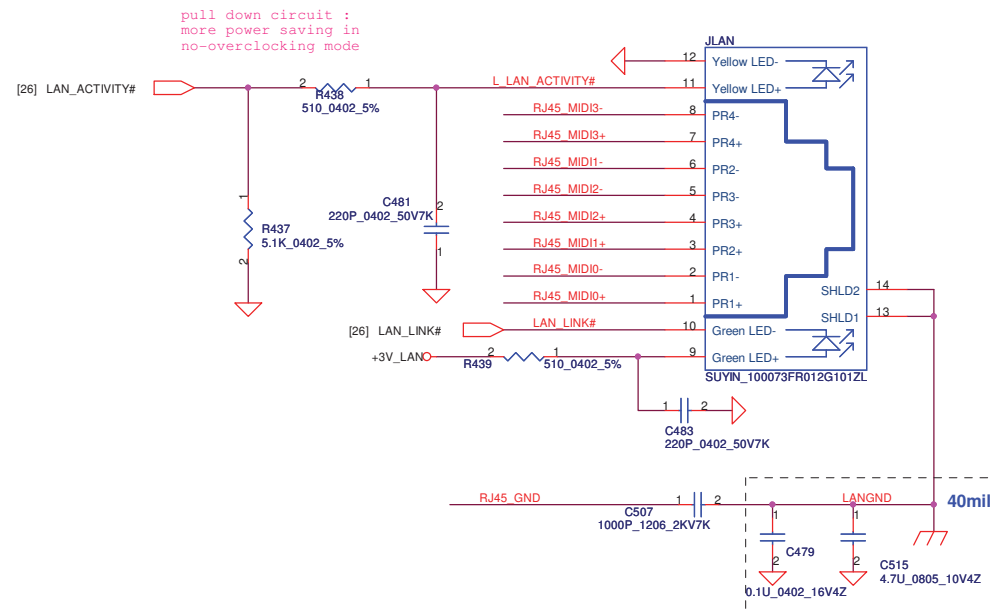
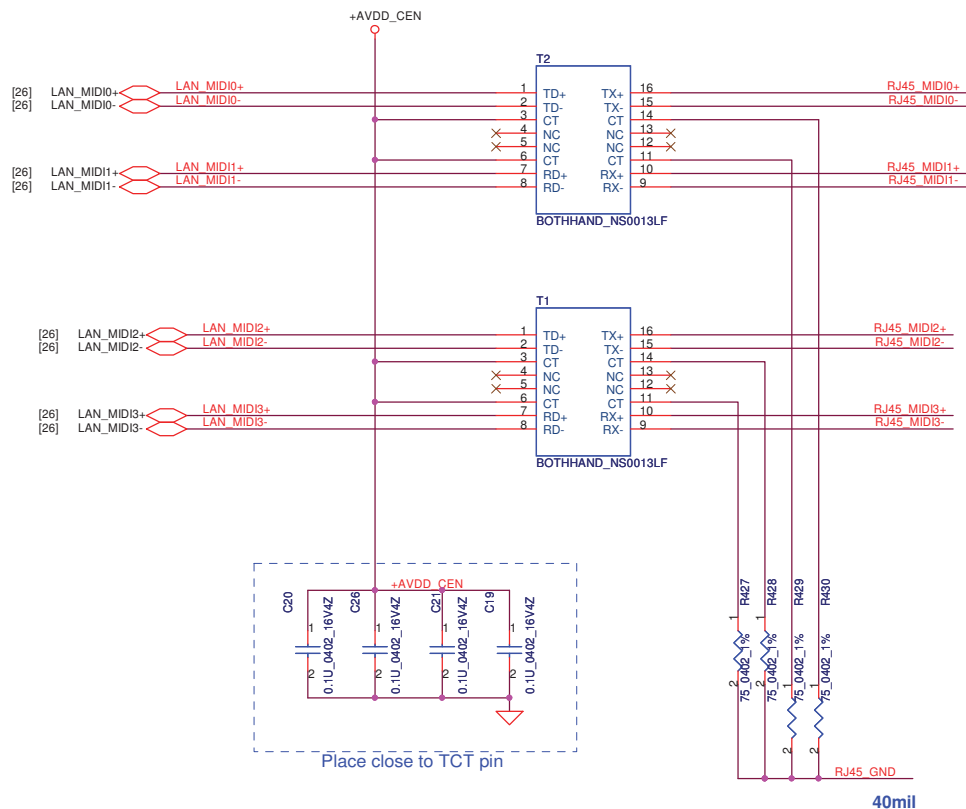
Intel Cantiga TMDs Pin Definition	
TMDs_B_CLK	PEG_TXP_3
TMDs_B_CLK#	PEG_TXN_3
TMDs_B_DATA0	PEG_TXP_2
TMDs_B_DATA0#	PEG_TXN_2
TMDs_B_DATA1	PEG_TXP_1
TMDs_B_DATA1#	PEG_TXN_1
TMDs_B_DATA2	PEG_TXP_0
TMDs_B_DATA2#	PEG_TXN_0
TMDs_B_HPD#	PEG_RXP_3



Place Close to Pin 2

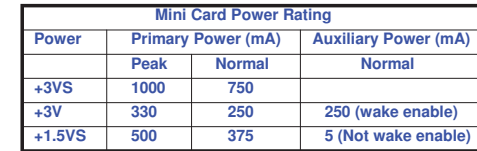


Place Close to LAN chip

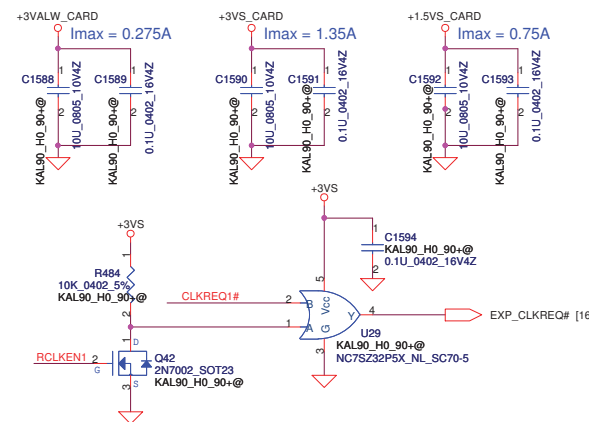


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Size	Document Number	Rev		Date	
B	KALG1	0.1		Tuesday, March 24, 2009	
Sheet		27		of 45	

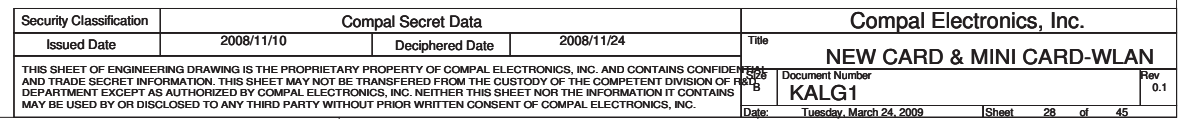
For Wireless LAN

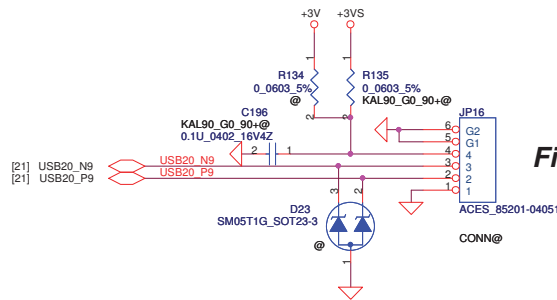


New Card Power Switch

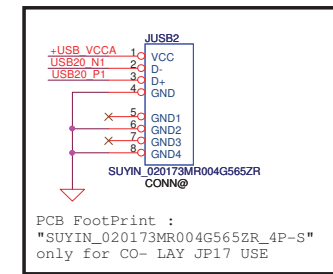


New Card Socket (Left/TOP)



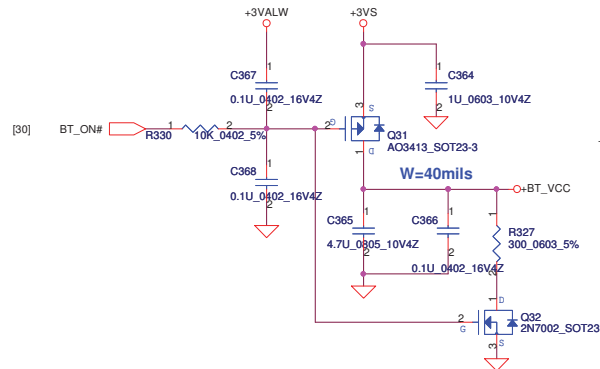


Finger Print Conn.

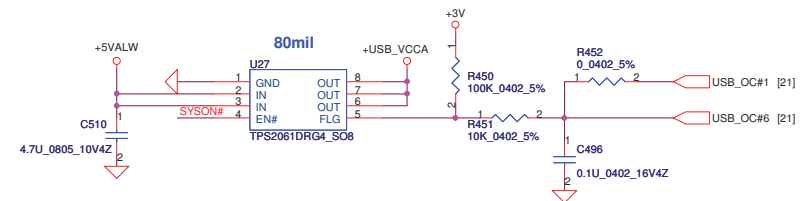
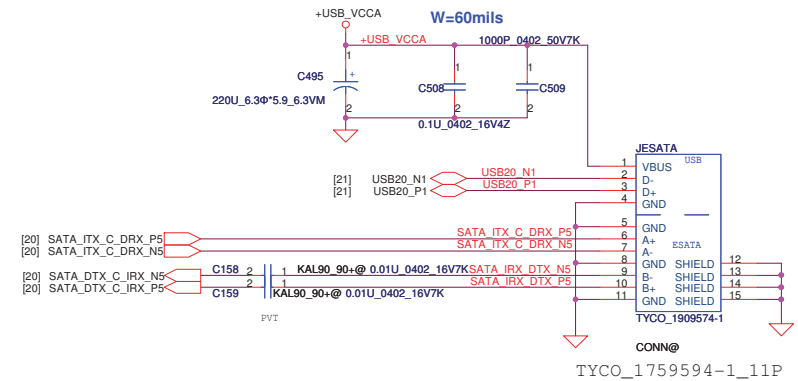
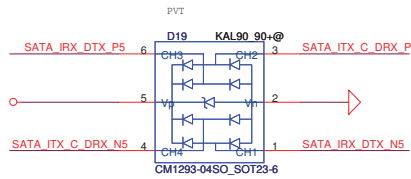
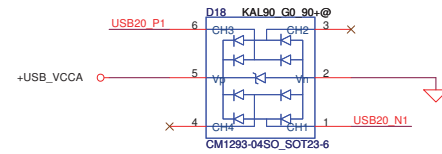


PCB FootPrint :
"SUYIN_020173MR004G565ZR_4P-S"
only for CO- LAY JP17 USE

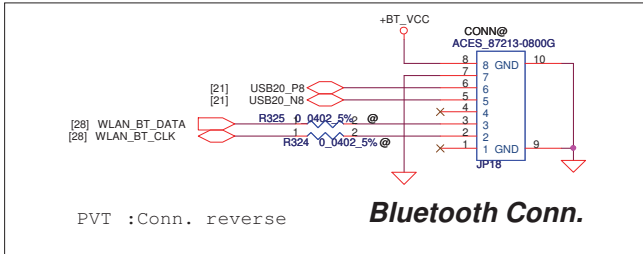
ESATA CONN



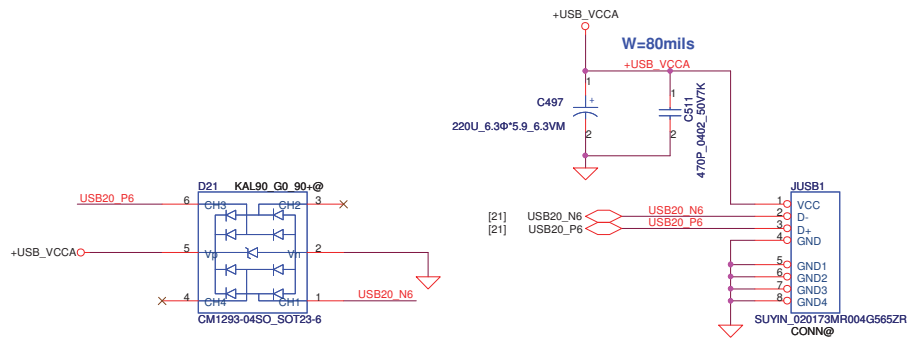
Bluetooth Conn.



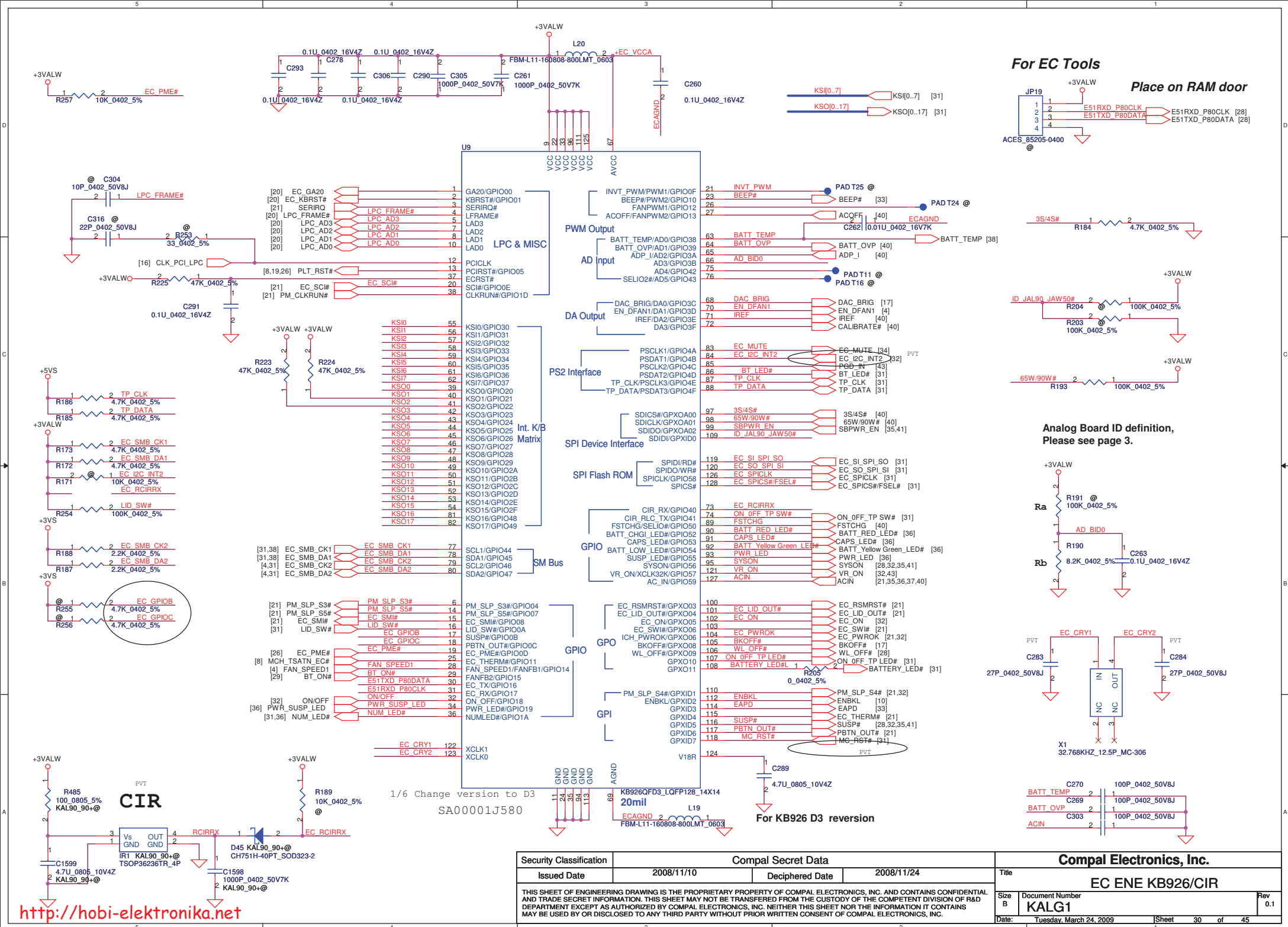
To USB/B Connector

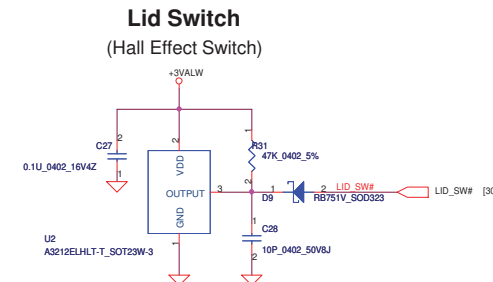
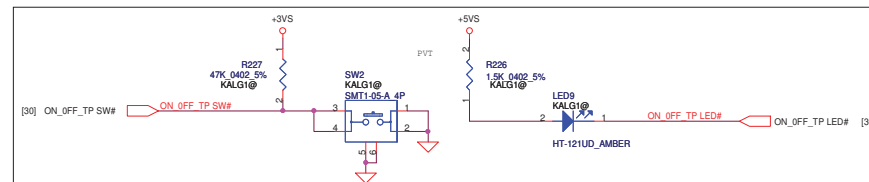
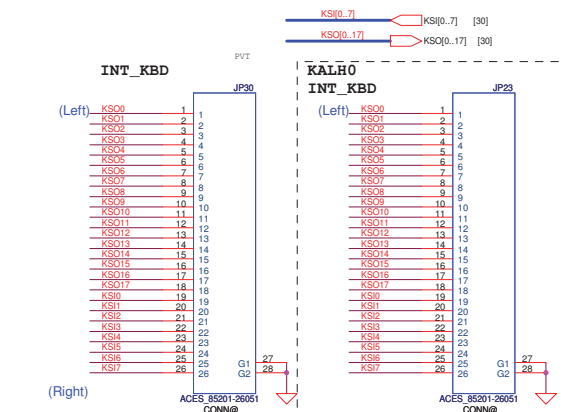
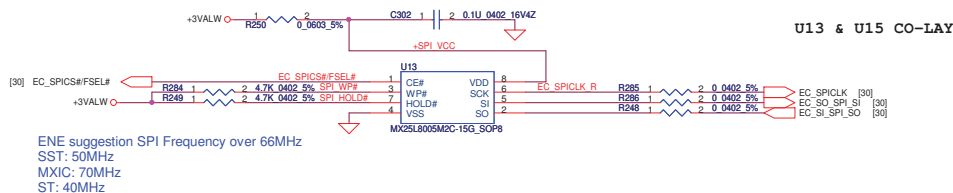


USB CONN.



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								Document Number				Rev	
								KALG1				0.1	
								Date				Tuesday, March 24, 2009	
								Sheet				29 of 45	

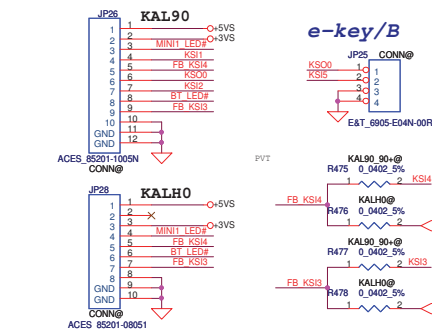
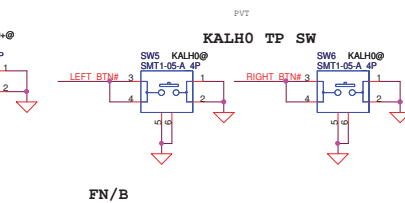
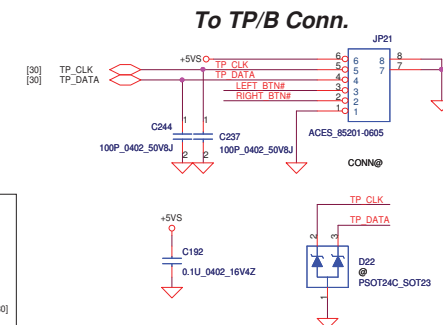




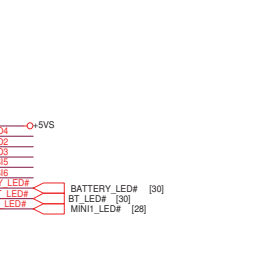
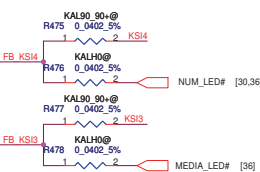
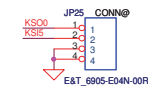
To BTN/B Conn.

	KSO0
KS11	WL_BTN#
KS12	BT_BTN#
KS13	EMAIL_BTN#
KS14	IE_BTN#
KS15	E-KEY_BTN#

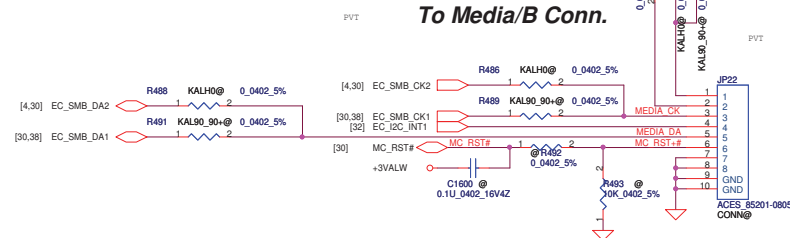
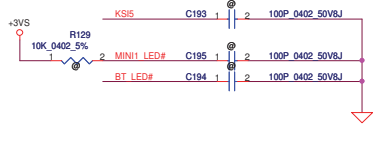
	KSO4	KSO2	KSO3
KS15	WL_BTN#	Volume Down	Back Up
KS16	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)



e-key/B

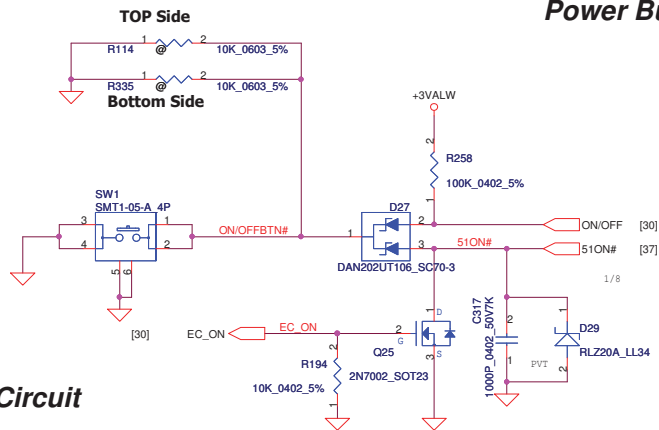


FOR EMI

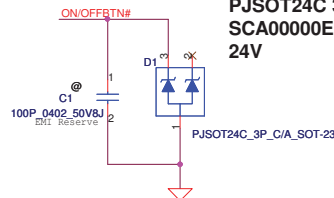


Security Classification	Compal Secret Data		Title	
Issued Date	2008/11/10	Deciphered Date	2008/11/24	BIOS, I/O Port & K/B Connector
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Date:	Tuesday, March 24, 2009	ISheet	31	of 45

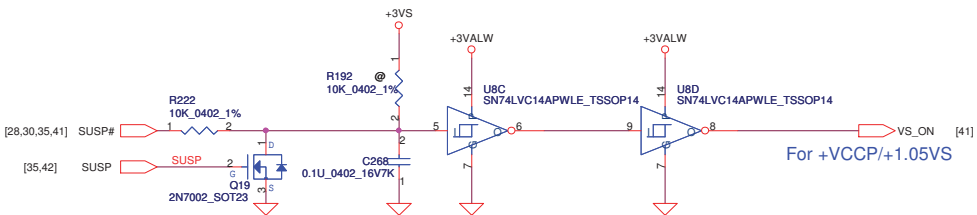
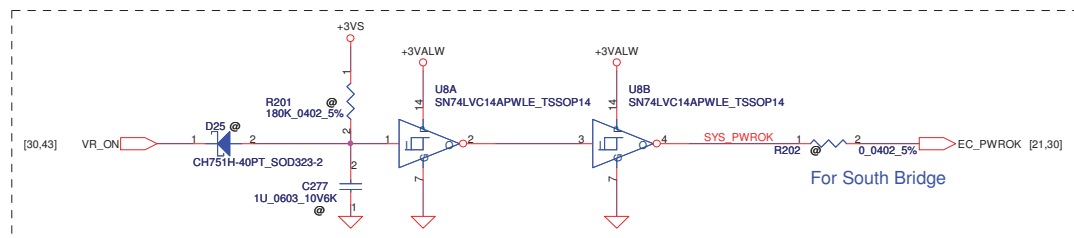
Power Button



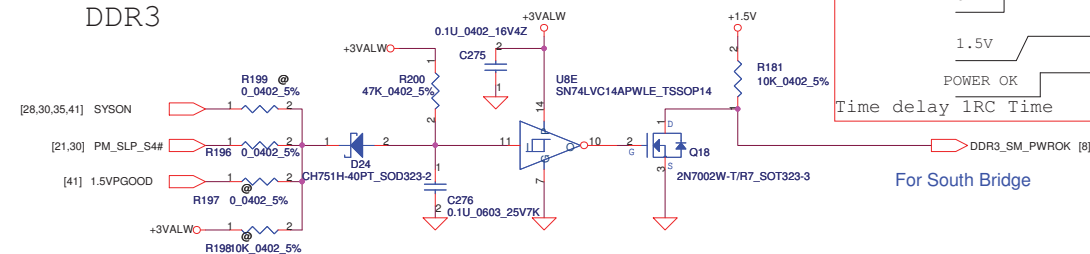
D58 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V



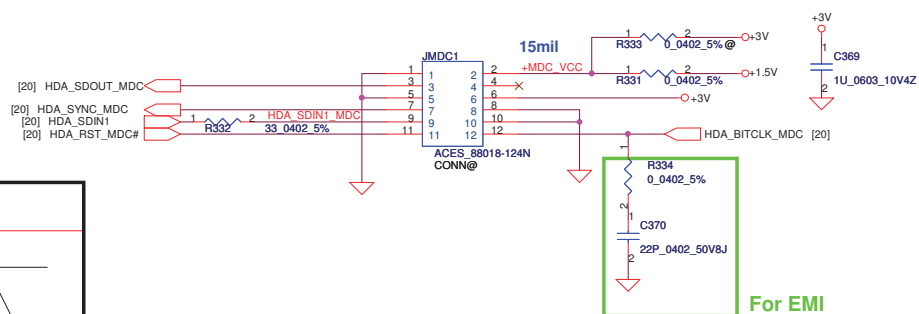
Power ON Circuit



DDR3



HDA MDC Conn.



For EMI

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				KALG1
				Rev 0.1
				Date: Tuesday, March 24, 2009
				Sheet 32 of 45

Gain= 10dB

Int. Speaker Conn.

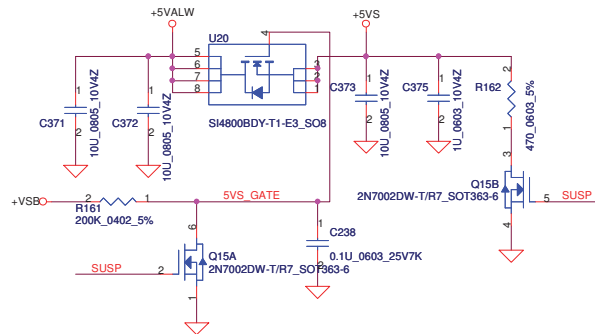
S/PDIF Out JACK
LINE Out/Headphone Out

(HDA Jack)
MIC JACK

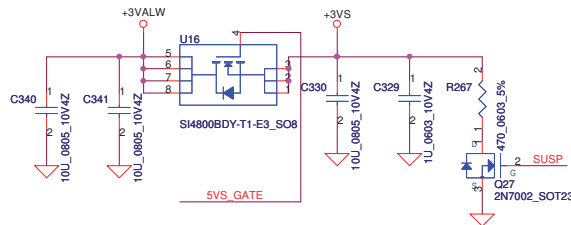
(HDA Jack)
LINE-IN JACK

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				Date Tuesday, March 24, 2009	Sheet 34 of 45

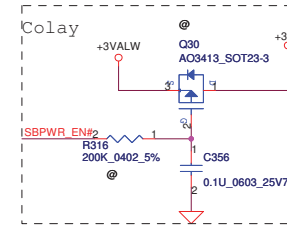
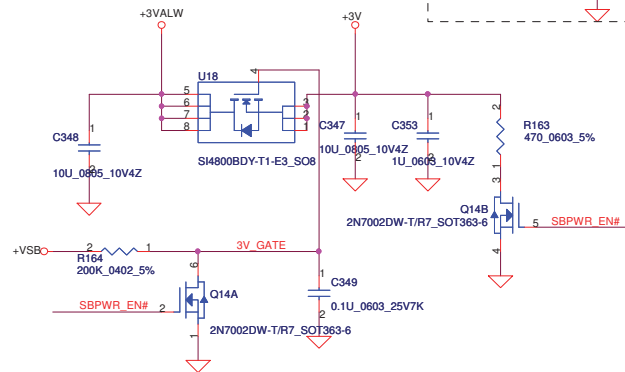
+5VALW TO +5VS



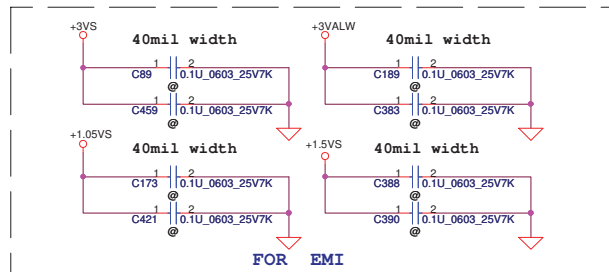
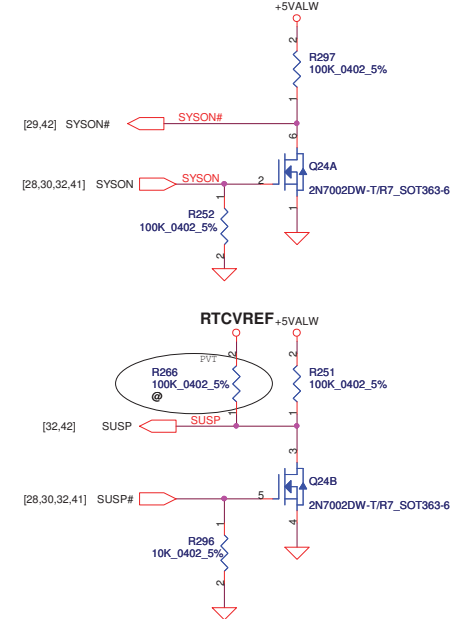
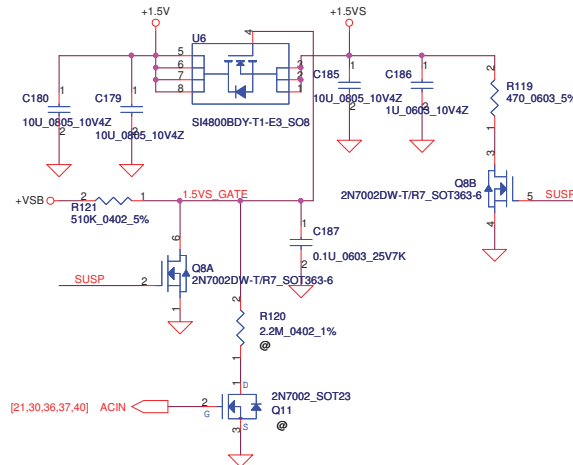
+3VALW TO +3VS



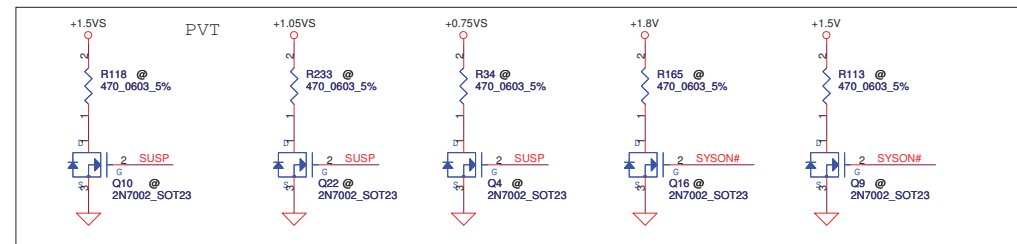
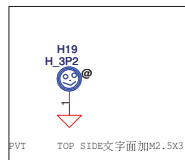
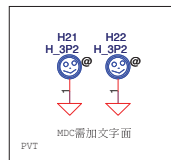
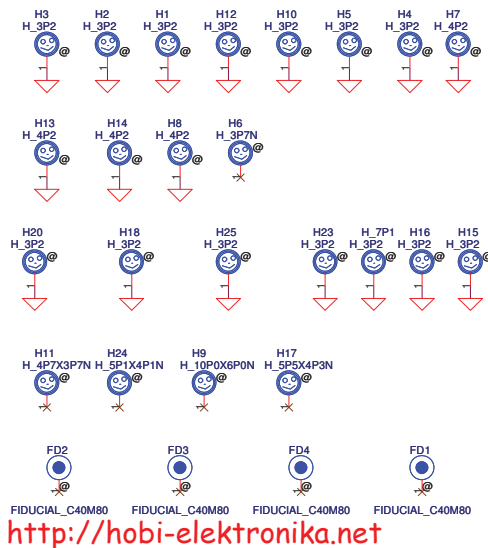
+3VALW TO +3V_SB(ICH8M AUX Power)



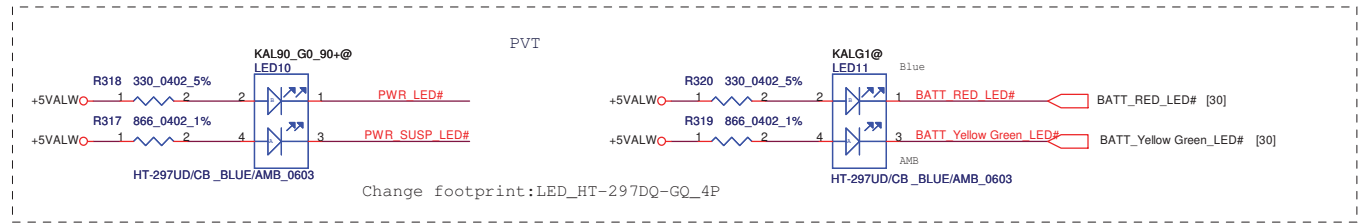
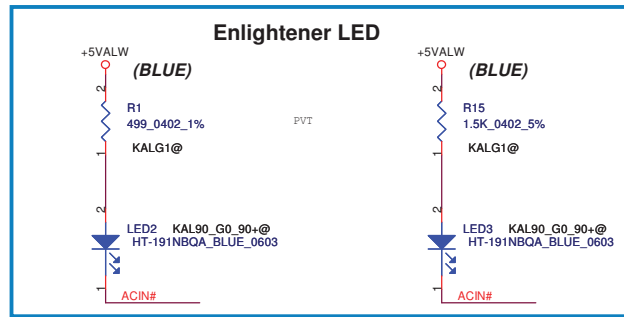
+1.5V to +1.5VS



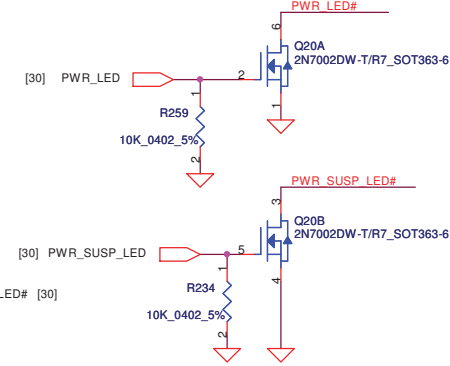
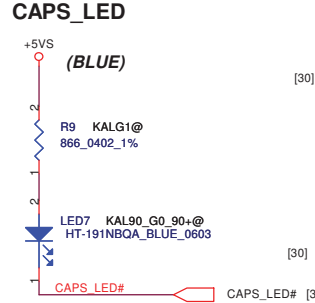
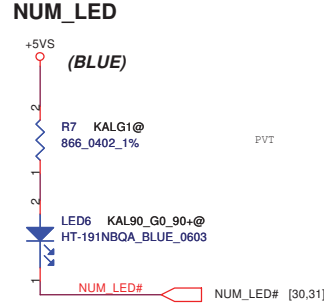
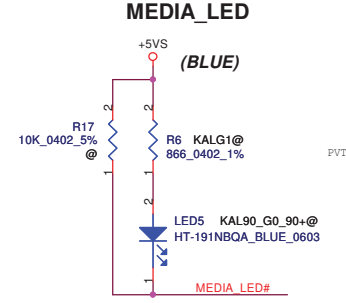
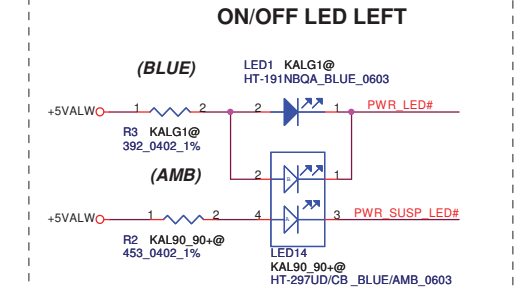
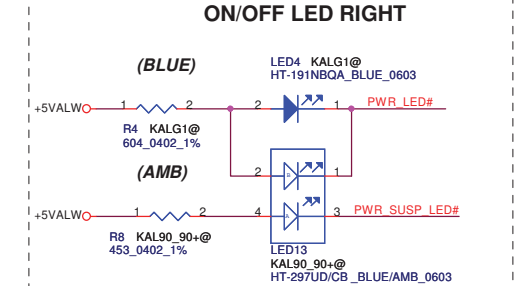
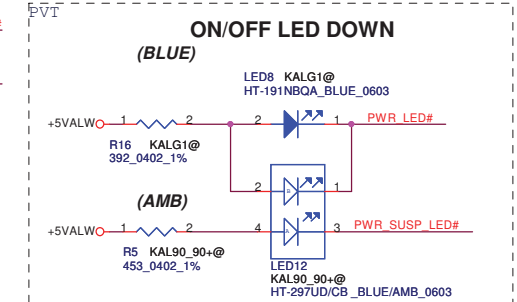
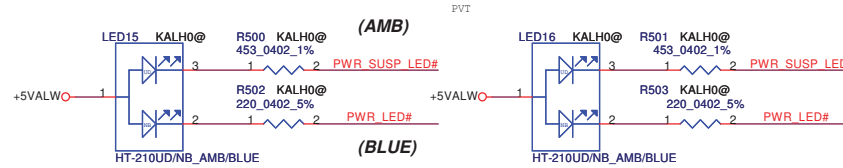
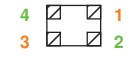
FOR EMI



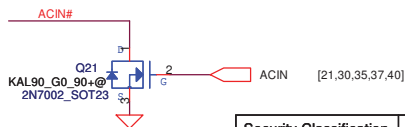
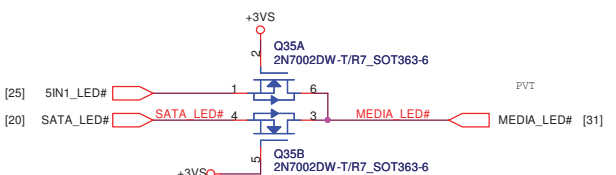
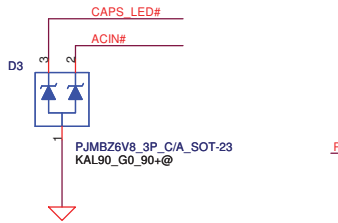
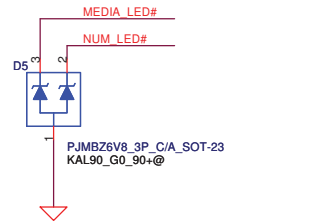
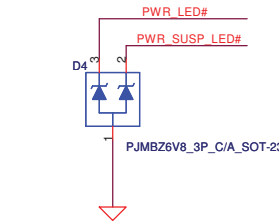
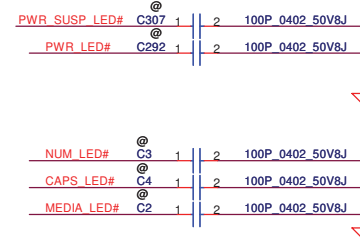
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Date: Tuesday, March 24, 2009				Document Number	Rev
KALG1				35	0.1
Sheet				35	45



Compal Footprint

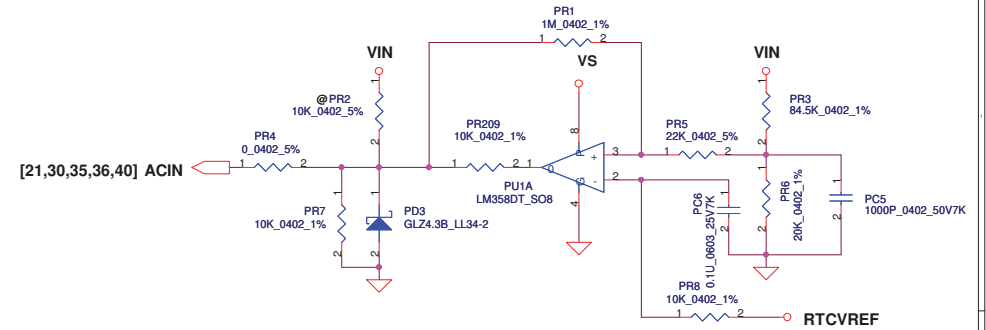
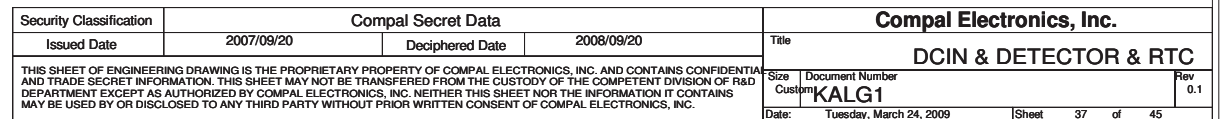
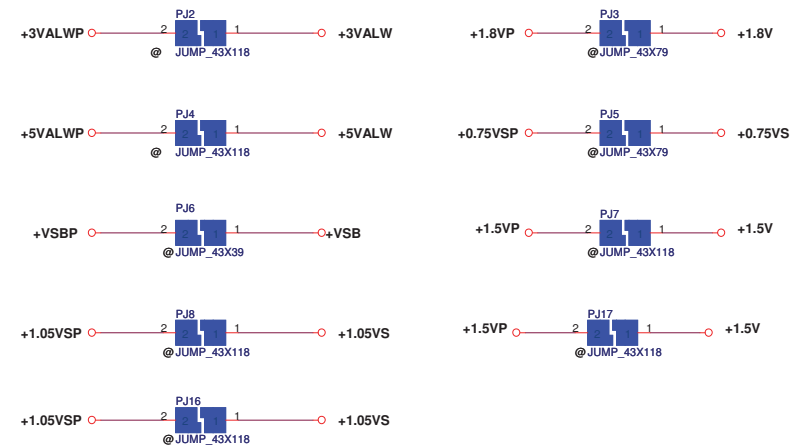


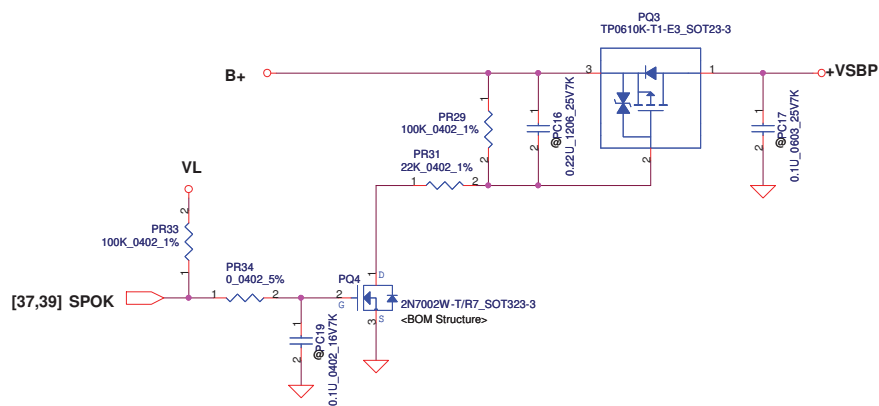
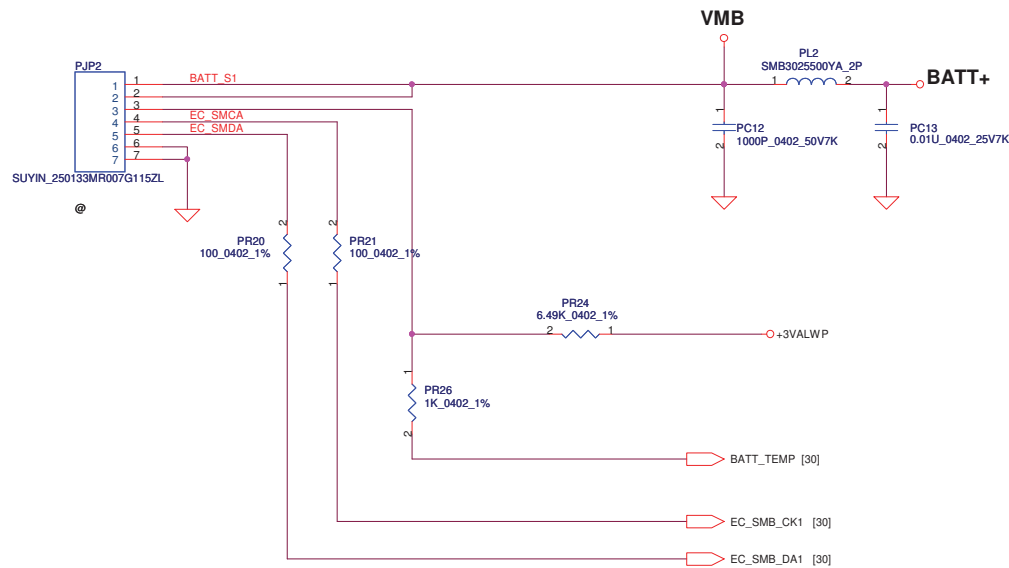
FOR EMI



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								Document Number			
								KALG1			
								Date			
								Tuesday, March 24, 2009			
								Sheet			
								36 of 45			

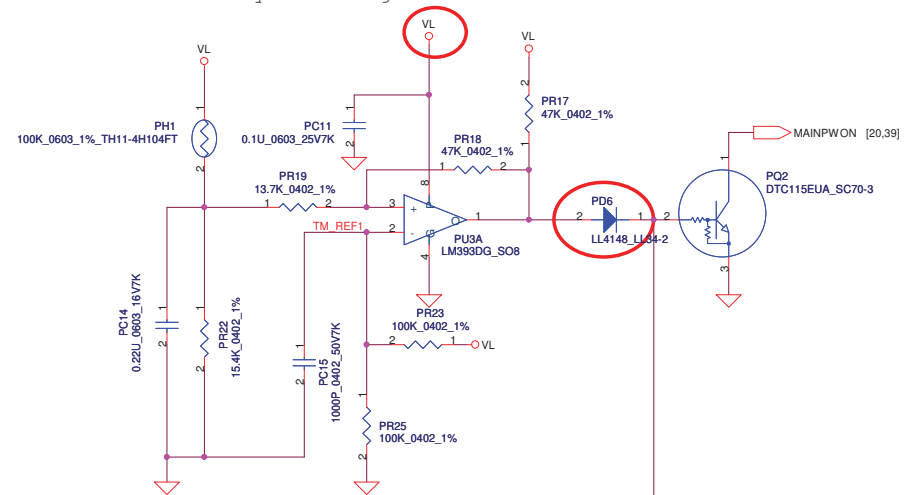
SINGA 2DC-G756I200

RTC Conn



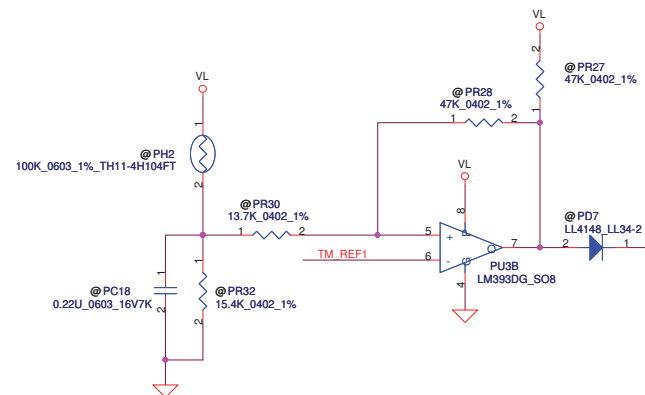
PH1 under CPU botten side :

CPU thermal protection at 96 degree C
Recovery at 60 degree C

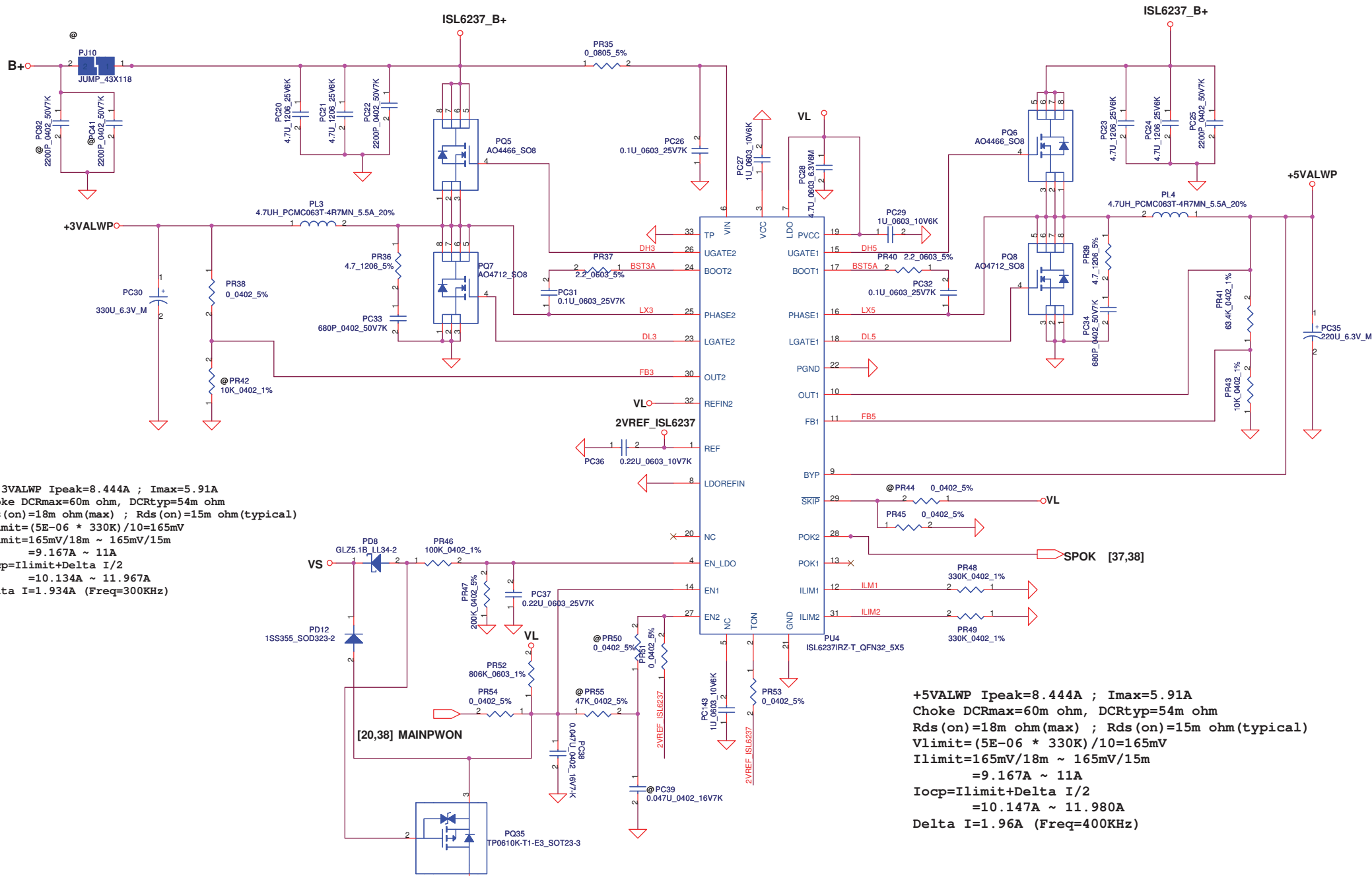


PH2 near main Battery CONN :

BAT. thermal protection at 79 degree C
Recovery at 47 degree C



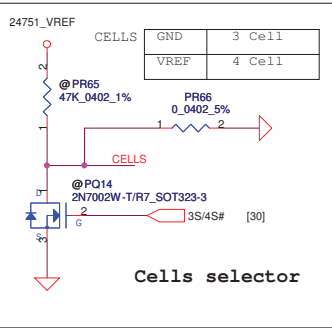
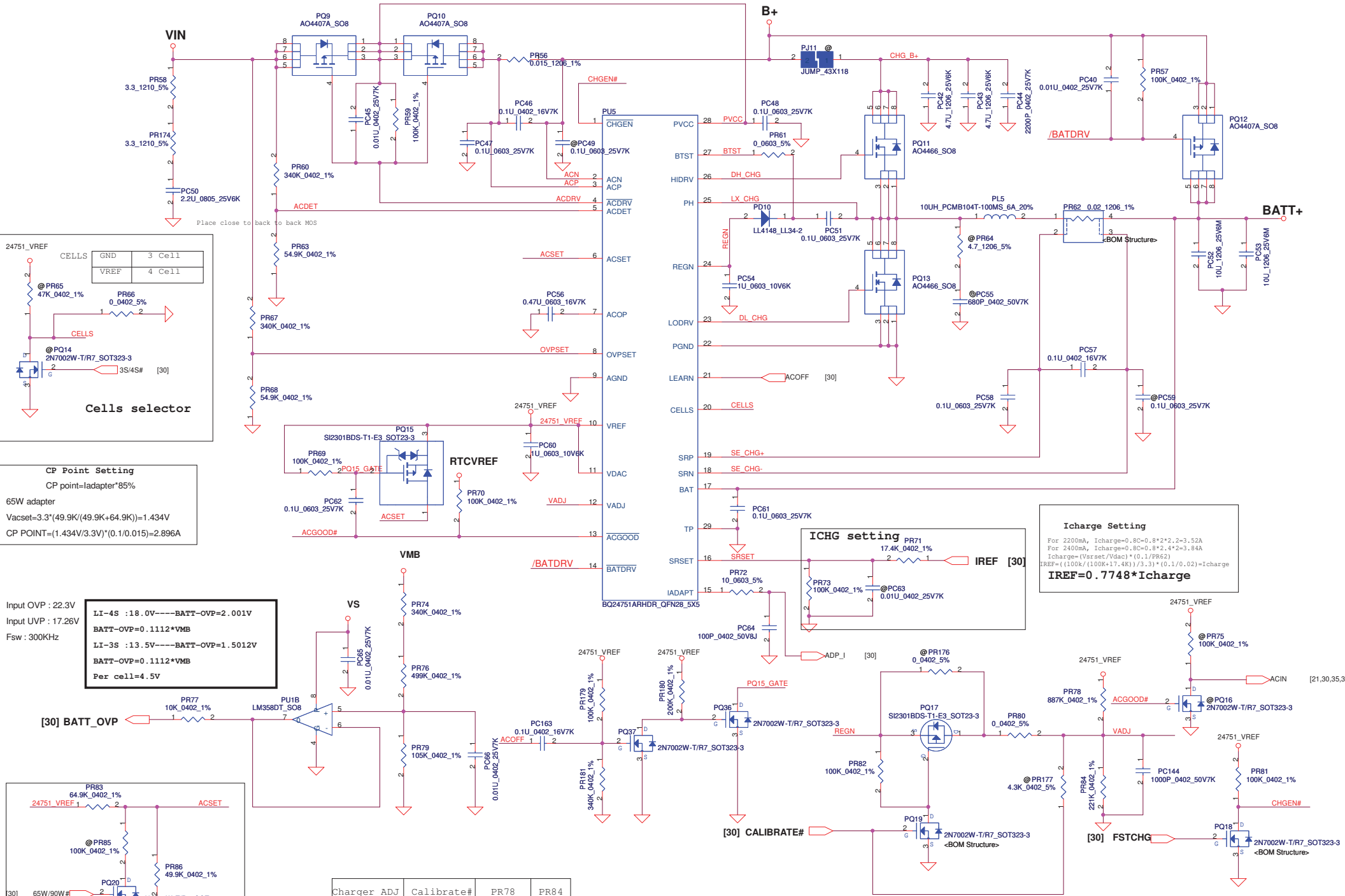
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				Custom	KALG1
				Date:	Tuesday, March 24, 2009
				Sheet	38 of 46
				Rev	0.1



+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 10.134A \sim 11.967A$
 $\Delta I = 1.934A$ (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 10.147A \sim 11.980A$
 $\Delta I = 1.96A$ (Freq=400KHz)

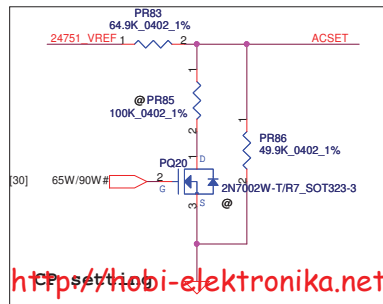
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Size	Custom	Document Number	KALG1	Rev	
Date:	Tuesday, March 24, 2009	Sheet	39	of 46	



CP Point Setting
 CP point=ladapter*85%
 65W adapter
 $V_{acset} = 3.3 * (49.9K / (49.9K + 64.9K)) = 1.434V$
 $CP\ POINT = (1.434V / 3.3V) * (0.1 / 0.015) = 2.896A$

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

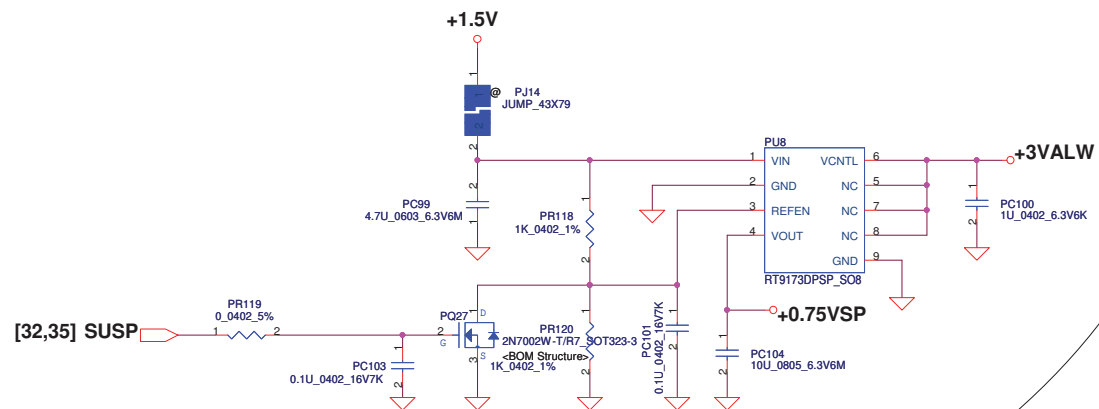
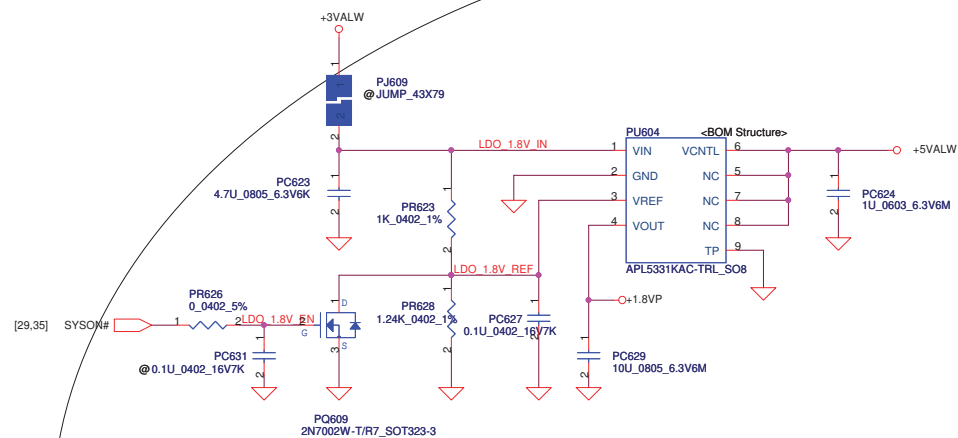
LI-4S : 18.0V----BATT-OVP=2.001V
 BATT-OVP=0.1112*VMB
 LI-3S : 13.5V----BATT-OVP=1.5012V
 BATT-OVP=0.1112*VMB
 Per cell=4.5V



Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@

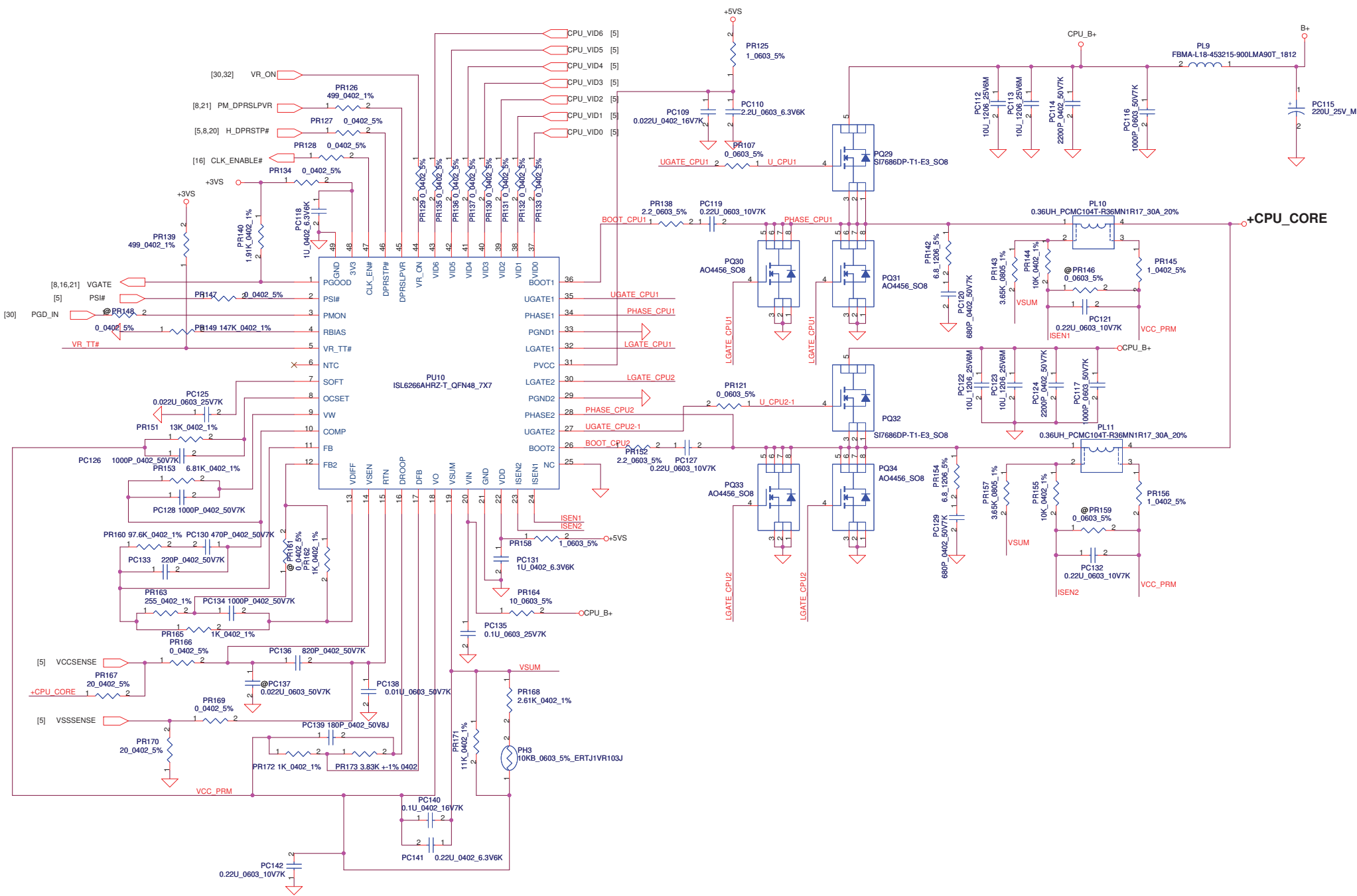
ICHG setting
 PR71 17.4K_0402_1%
 PR73 100K_0402_1%
 @PC63 0.01U_0402_25V7K

Icharge Setting
 For 2200mA, Icharge=0.8*0.8*2*2.2=3.52A
 For 2400mA, Icharge=0.8*0.8*2.4*2=3.84A
 $I_{charge} = (V_{set} / V_{dca}) * (0.1 / PR62)$
 $IREF = ((100K / (100K + 17.4K)) / 3.3) * (0.1 / 0.02) = I_{charge}$
IREF=0.7748*Icharge



12/25

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				Custom
				Document Number
				KALG1
				Rev
				0.1
				Date
				Tuesday, March 24, 2009
				Sheet
				42 of 46



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	+CPU_CORE
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Size	Custom	Document Number	KALG1	Rev	0.1
Date:	Tuesday, March 24, 2009	Sheet	43	of	46

Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add 3/5V boost resister for EMI request			Change PR37 and PR40 to 2.2 OHM		
2		Modify 1.5V and 1.05V choke to cyntec for eff.			PL501 & PL502		
3		Modify 1.5V and 1.05V frequnce from 336K to 264K for eff.			Change PR525 & PR501 from 240K to 300K		
4		Modify 1.5V and 1.05V low side mos for eff.			Change PQ506 & PQ508 from FDS6670 to A04456		
5		Add CPU_core boost resister for EMI request			Change PR138 and PR158 to 2.2 OHM		
6		Modify 1.5V & 1.05V OCP to 14A			Change PR530 & PR522 to 5.9K		
7		Modify 3V & 5V choke to 4.7UH for eff.			Change PL3 & PL4 from 8.2UH to 4.7UH		
8		Modify 5V output cap to OS-CON for costdown			Change PC35		
9		Modify 3V output cap to OS-CON for costdown			Change PC30		
10		Modify dischager mos to A04407A for rating risk			Change PQ12		
11		Add 30K OHM to TPS51117 EN pin , Disable SMPS mode			ADD PR910 & PR911		
12							
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				Size Custom	Document Number KALG1
Date: Tuesday, March 24, 2009		Sheet 44 of 46			

PCB



LA-5271P MB Rev0: DA60000C500

PCB 08Y LA-5271P REV0 M/B

North Bridge



PVT
GL40: SA00002Q8N0

S IC AC82GL40 SLGGM A1 FCBGA1329 GL ABO
GL40@

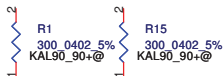
MEDIA_LED NUM_LED CAPS_LED



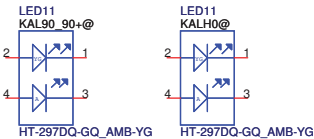
ON/OFF LED Risiter



Enlightener LED



Page 36



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							Size	Document Number		Rev		
							Custom	KALG1		0.1		
							Date:		Tuesday, March 24, 2009		Sheet 46 of 46	